

Epson Timing Device

FY2025

Epson Europe Electronics Munich
Industry

**Epson IMU positioning
test with Novatel
(2023)**



**Seiko Astron, World's
First Quartz Wristwatch
(1969)**



home

Seiko Epson Corporation

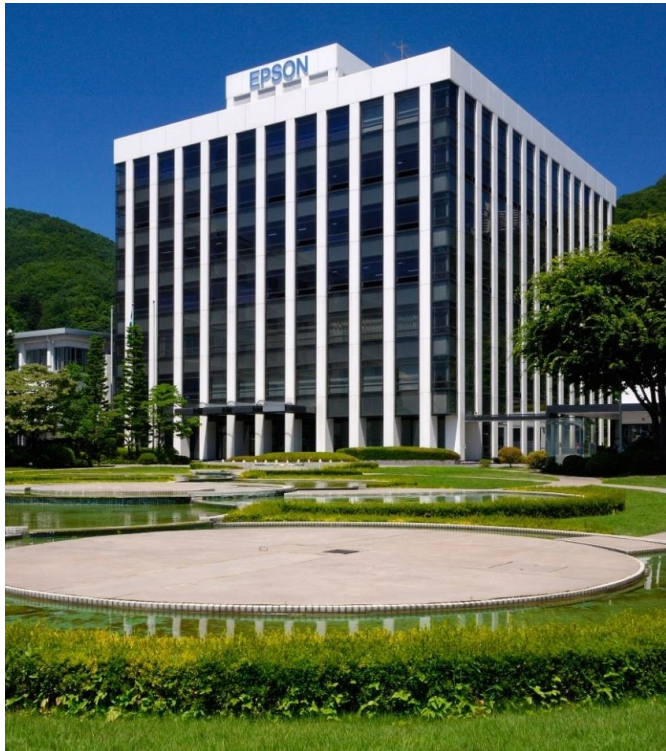
- Company & Epson Timing Devices
- Epson Core Technology

Key Products

- kHz and MHz Crystal
- Real Time Clock Module
- SPXO / TCXO
- High end SPXO / TCXO / VCXO for Networking
- Clock Buffers 
- Automotive Grade for Industry

Appendix

- Useful links



SEIKO EPSON HQ, Suwa, Nagano, Japan



Yasunori Ogawa
President

Microdevices
Revenue

\$ 717 M (FY2023)



79,944
Employees



83 Group
Companies

Founded 1942



Revenue (consolidated)
\$9.17 B (FY2023)

Business Profit (consolidated)
\$ 517 M (FY2023)

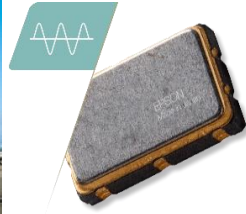
HQ - Ina,
Japan



Fab -
Sakata,
Japan

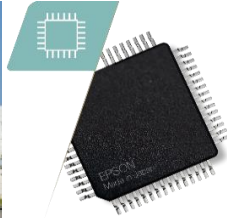


Fujimi,
Japan



“TD” Timing Devices

Quartz Crystals, Oscillators, RTCs, Gyros
Used in Seiko watches and all Epson products



“IC” Semiconductor Products

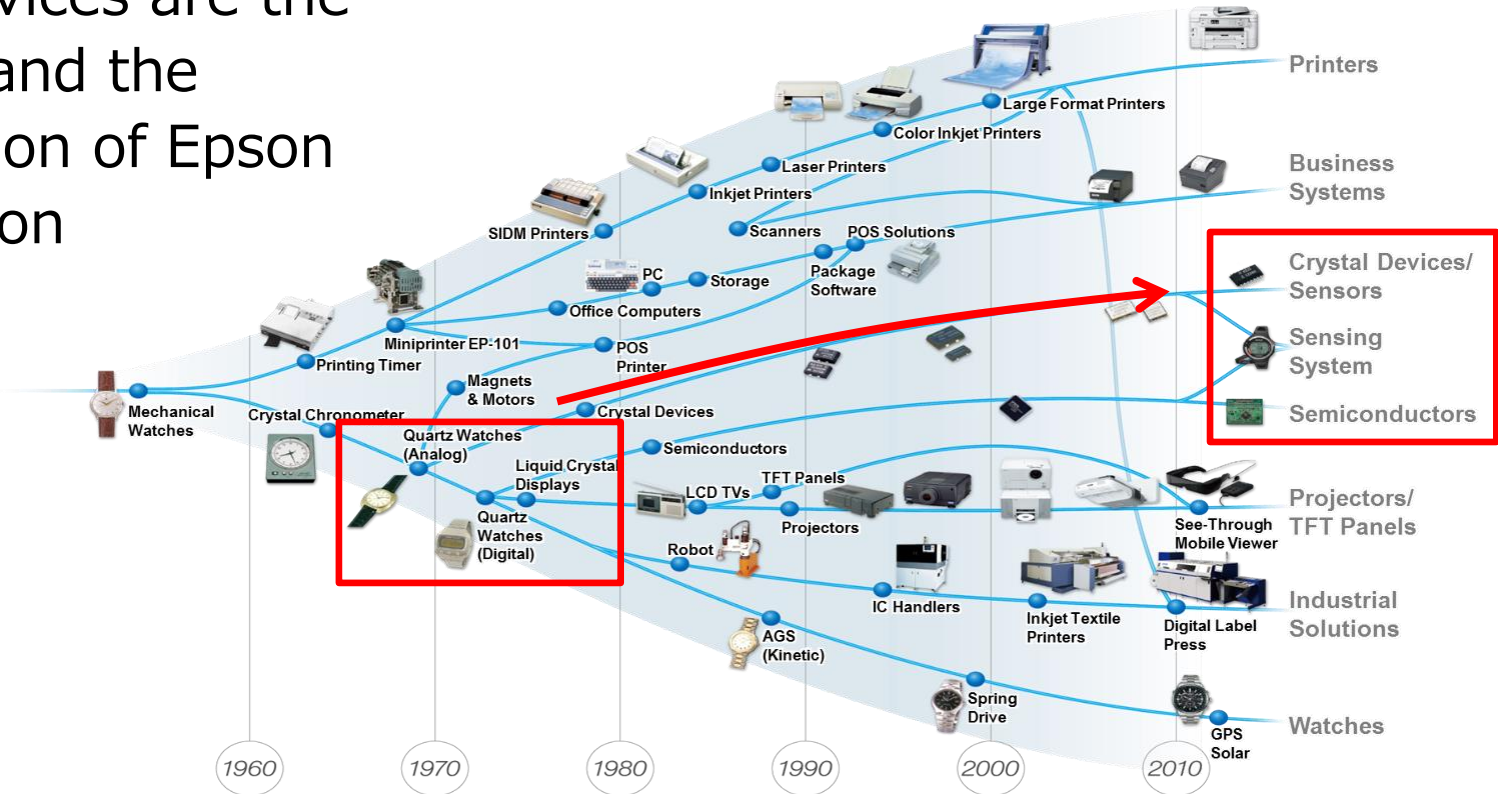
Microcontrollers, LCD controllers, PMICs, etc
Used in Epson printers and projectors



“IMU” Inertial Sensors

Gyros & IMUs
Used in Epson robots

Microdevices are the history and the foundation of Epson innovation



Seiko Epson Corp. Revenue Split

EPSON

Revenue (Consolidated)

FY2023

¥1,313.9 billion

Business Profit (Consolidated)

FY2023

¥64.7 billion

* Business profit is very similar to operating income under Japanese accounting standards, both conceptually and numerically. It is calculated by deducting the cost of sales and selling, general and administrative expenses from revenue.

Segment Revenue as a Percentage of Total Revenue

(FY2023)

Manufacturing-Related & Wearables

13.7%

16.5%

Visual Communications

Commercial &
Industrial
Printing

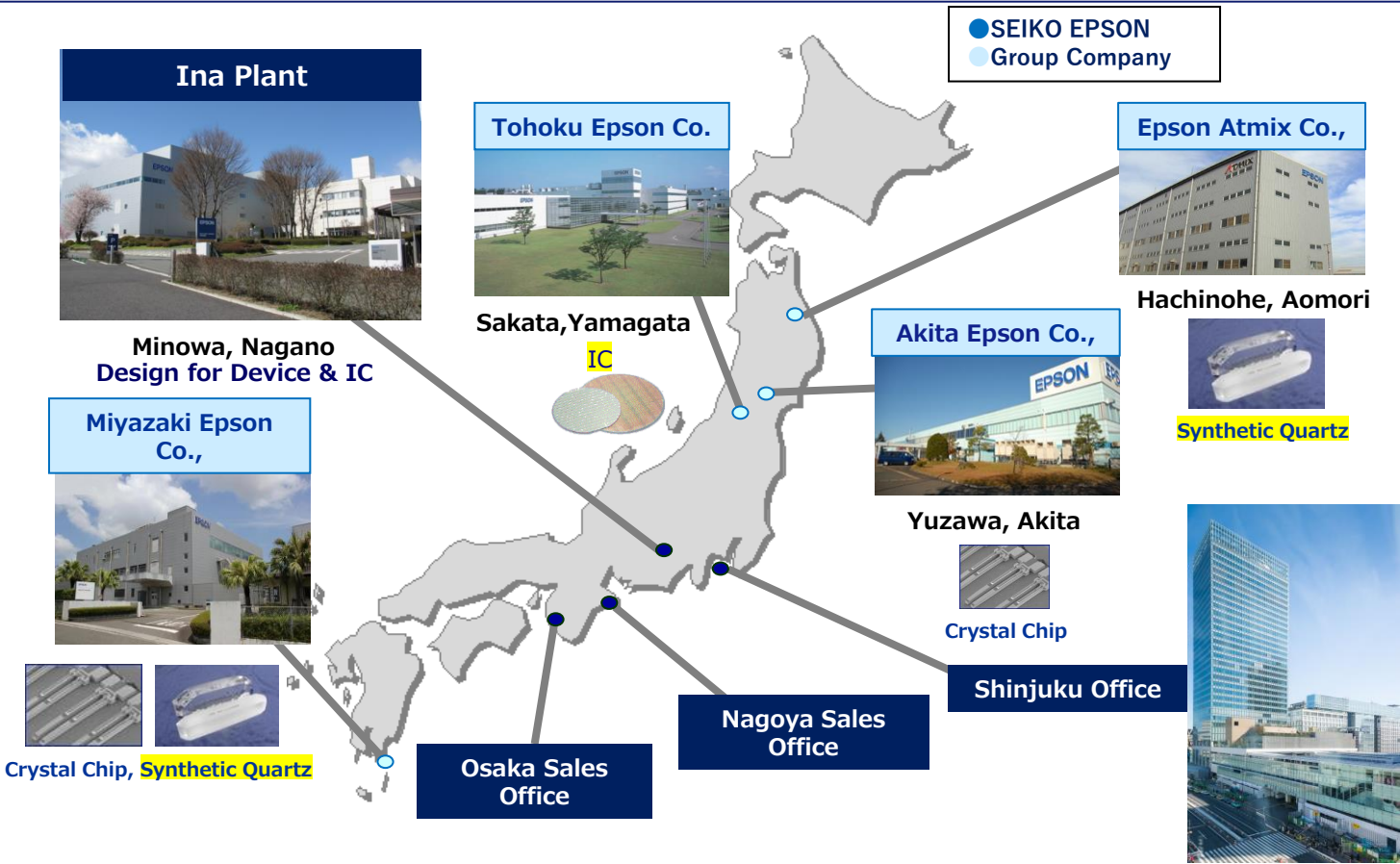
69.8%
Printing
Solutions

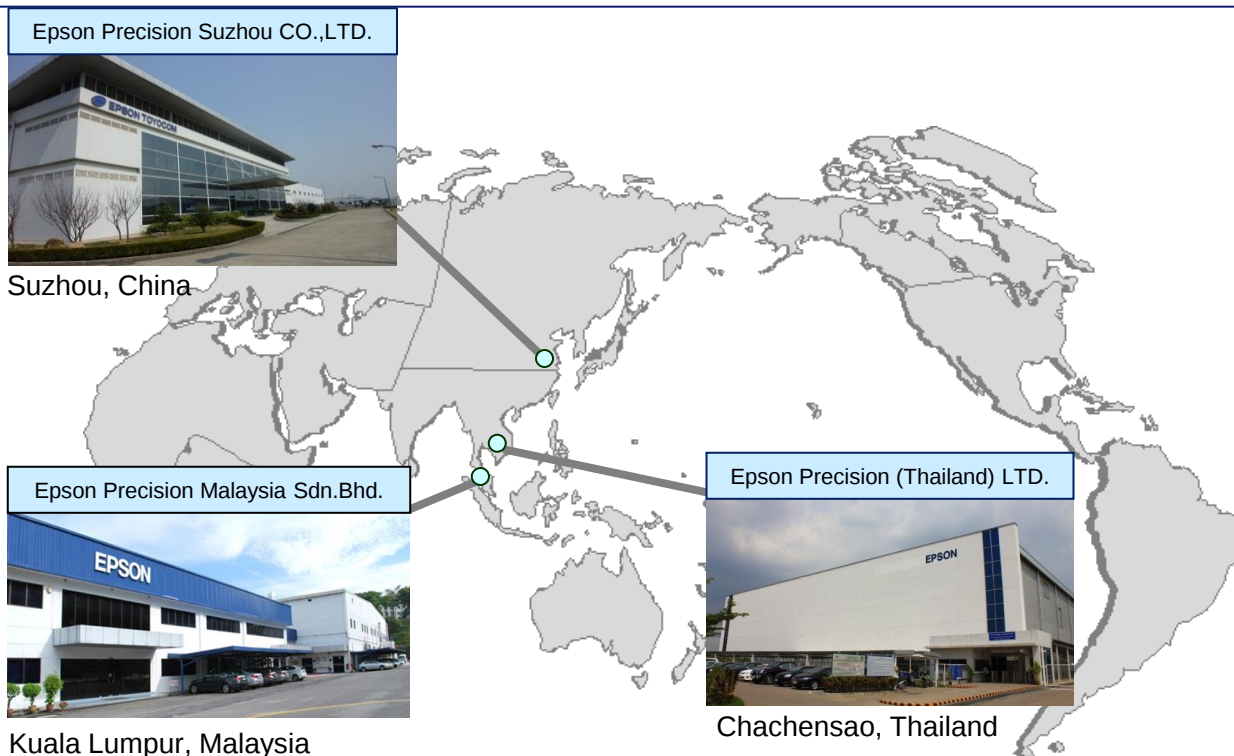
Office & Home
Printing

Innovation	Office & Home Printing Innovation		Commercial & Industrial Printing Innovation	Visual Innovation	Manufacturing Innovation	Lifestyle Innovation		
Segment	Printing solutions business			Visual communications business	Manufacturing-related & wearables business			
Operation	Office & home printing business		Commercial & Industrial printing business	Visual communications business	Manufacturing solutions business	Wearable products business	Microdevices business	PC business
Main Technology	Micro Piezo inkjet technology Dry Fiber Technology			Microdisplay technology Projection technology	Precision mechatronic technology High-precision sensing technology Software technology Ultra-precision & micromachining technology High-density board assembly technology Low power consumption technology			
Main Operations	Office & home inkjet printers, serial impact dot matrix(SIDM) printers, page printers, color image scanners, dry process office papermaking systems, and related consumables		Commercial & industrial inkjet printers, inkjet printheads, printers for use in POS systems, label printers, and consumables	Projectors and smart glasses	Industrial robots, micro injection molding machines	Wristwatches, watch movements	Crystal devices (crystal units, oscillators, sensors) Semiconductors (CMOS, LSI), Superfine alloy powder Surface finishing	PCs & other
Global Market Share	Inkjet printers (unit volume)¹ No.2 32%  Printer market (including laser printers, unit volume)² No.3 20%  Projectors (>500 lumens, unit volume)³ No.1 51%  SCARA robots (unit volume)⁴ No.1 21%  Crystal oscillators (sales revenue)⁵ 24% 							

1 Source: IDC's Worldwide Quarterly Hardcopy Peripherals Tracker 2024Q1 Share by Brand 2 Source: IDC's Worldwide Quarterly Hardcopy Peripherals Tracker 2024Q1 Share by Brand. Laser printers = up to 90 ppm monochrome laser printers. Color laser = up to 69 ppm 3 Unit volume share for projectors with 500 lumens or more, excluding screenless TV products. Source: Futuresource Consulting Ltd., FY2023 4 Source: Epson documents based on Fuji Keizai's "Current status and future outlook of worldwide robot-related markets 2024" 5 Source: QYRESEARCH Inc. Global Timing Device Market Report, published 2023

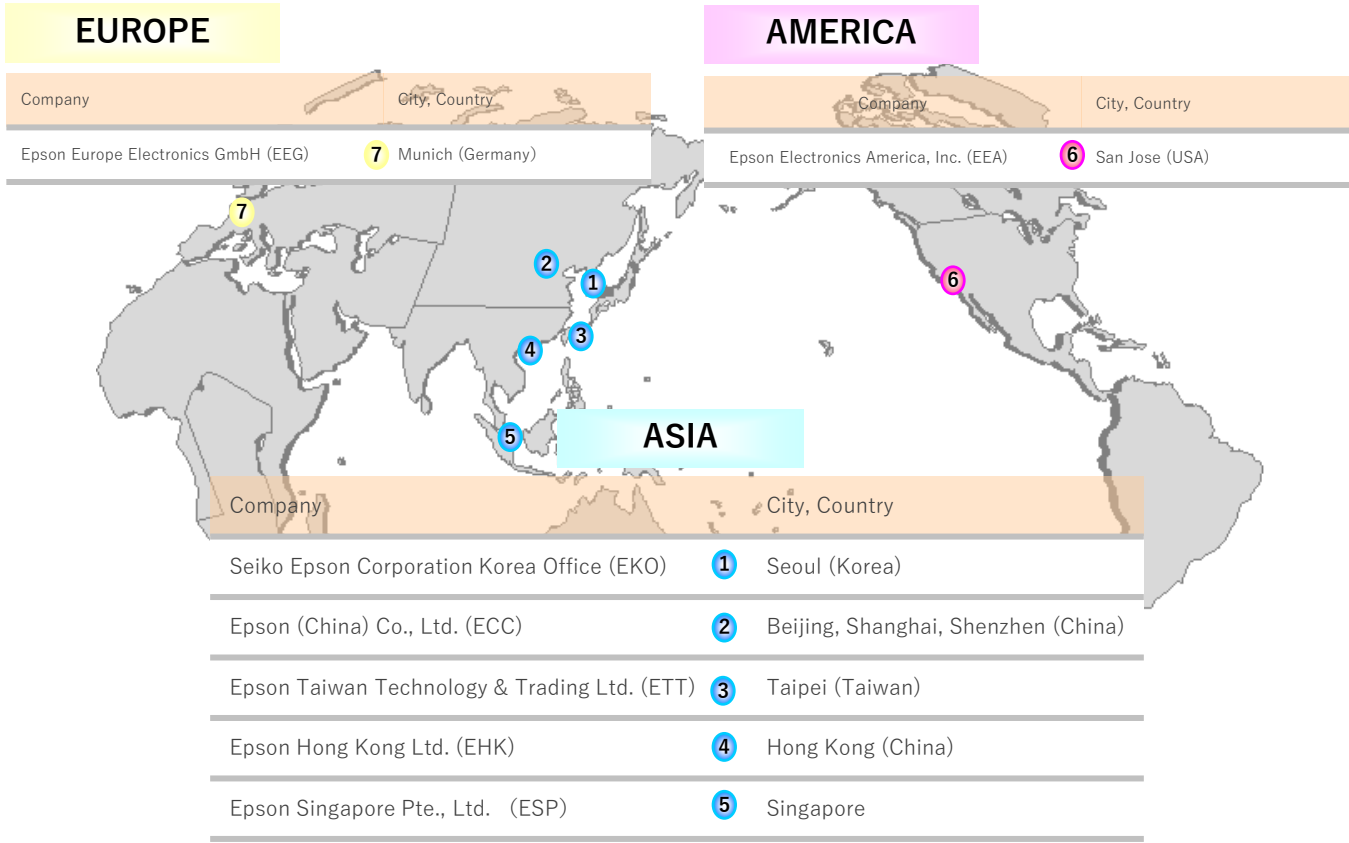
Domestic Plants and Offices (Japan)





- flexible sites and production lines
- maximum of supply security and capacity

home





See more

Environmental Vision 2050
<https://global.epson.com/SR/environment/vision/>

Epson will become carbon negative and underground resource^{*1} free by 2050 to achieve sustainability and enrich communities

^{*1} Non-renewable resources such as oil and metals

Goals

- 2030: Reduce total emissions in line with the 1.5° C scenario^{*2}
- 2050: Carbon negative and underground resource^{*1} free

Actions

- Reduce the environmental impacts of products and services and in supply chains
- Achieve sustainability in a circular economy and advance the frontiers of industry through creative, open innovation
- Contribute to international environmental initiatives

^{*1} Non-renewable resources such as oil and metals

^{*2} Target for reducing greenhouse gas emissions aligned with the criteria under the Science Based Targets initiative (SBTi)

1) Utilization of renewable energy (Installation of solar power generation equipment))

Installations in Ina, Thailand, China crystal business bases.
Installations & expansions at two domestic bases by the end of FY2022
Installation at Malaysian crystal business base by the end of FY2023



Left: Thailand, Right: China

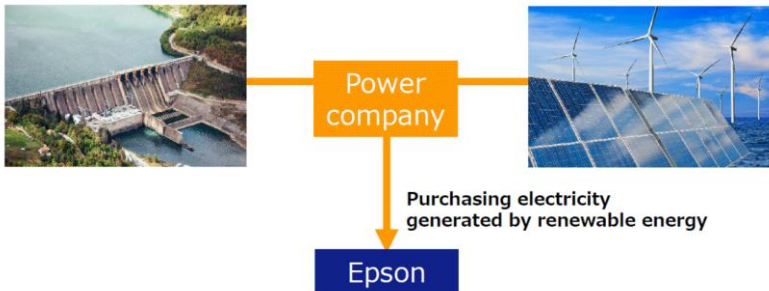
2) Environmental investment in line with maintenance and renewal of basic equipment

High-efficiency HVAC system improvements at Overseas base of crystal business by the end of FY2023
- Aged air conditioning system, piping renewal
- Optimization of piping and wiring layout



3) Purchase of Carbon-free electricity (Renewable energy)

Crystal Business at our domestic bases uses electricity which converted into 100% renewable energy.
We plan to convert the electricity used at all crystal business bases to renewable energy by the end of 2023
*Some rental properties such as sales bases are excluded.



ESG Indices and Ratings Inclusion

https://global.epson.com/SR/evaluation/?fwlink=sr_top

In green: After Jan. 2022

- FTSE4Good Index Series: 18th consecutive year
- FTSE Blossom Japan Index (GPIF adopted index): 5th consecutive year
- **FTSE Blossom Japan Sector Relative Index** (GPIF adopted index): first time
- Empowering Women Index (WIN) (GPIF adopted index): 5th consecutive year
- S&P/JPX Carbon Efficient Index (GPIF adopted index): 4th consecutive year
- Sompo Sustainability Index: 10th consecutive year
- CDP A Lists (climate change and water security): 2nd Consecutive Year
- **CDP Supplier Engagement Rating Leaderboard: 3rd Consecutive Year**
- EcoVadis Platinum Rating for Overall Sustainability: 2nd Consecutive Year
- **DBJ (Development Bank of Japan) Environmentally Rated Loan Program Rank A: first time**



FTSE4Good



FTSE Blossom Japan



ESG awards / Index Adoption

- Forbes JAPAN Ranked No.1 in “The 100 Most Sustainable Companies”: Sep. 2021
- 3rd Annual SDGs Management Survey top-rated level: Nov. 2021
- Environmental Value Award at the 3rd Annual Nikkei SDGs Management Grand Prix: Nov. 2021
- **Silver Award in the Environmentally Sustainable Company category of the third ESG Finance Awards Japan: Feb. 2022**
- **2022 Health & Productivity Stock Selection (No.1 in electrical equipment) *: March 2022**
- Nikkei 225: from 2017

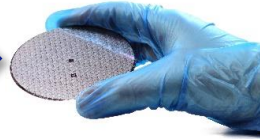
*Health Management Objectives and Organization
https://global.epson.com/SR/our_people/health_and_productivity.html#h2_02





IC Design

Epson is 1 of very few who design their own ICs



IC Fabrication

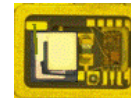
Epson is the only supplier with our own IC foundry



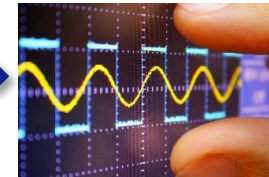
Epson is the only supplier who makes their own robots



Module Assembly



Crystal and IC inside ceramic package



Final Test

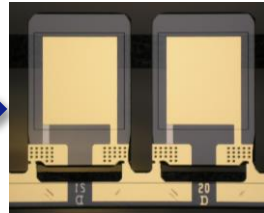


100% tested



Synthetic Quartz

Epson is 1 of few suppliers who grow their own Quartz



Crystal Fabrication

Epson was the 1st to develop Photolithographic Quartz crystals



EXPLAINER VIDEO



Epson timing products - manufacturing process

Core Technology - Synthetic Quartz Production

EPSON



2-6
months



- Hachinohe, Aomori, Japan
- Miyazaki, Japan
- Longmont, WA



Natural Quartz

Better Purity

Lower Defects



Synthetic Quartz

World's Largest
Autoclaves

16 Autoclaves
in 2 locations

Assurance of
Supply

Lower Defect
Density

Enhanced
Stability

Improved
Phase Noise

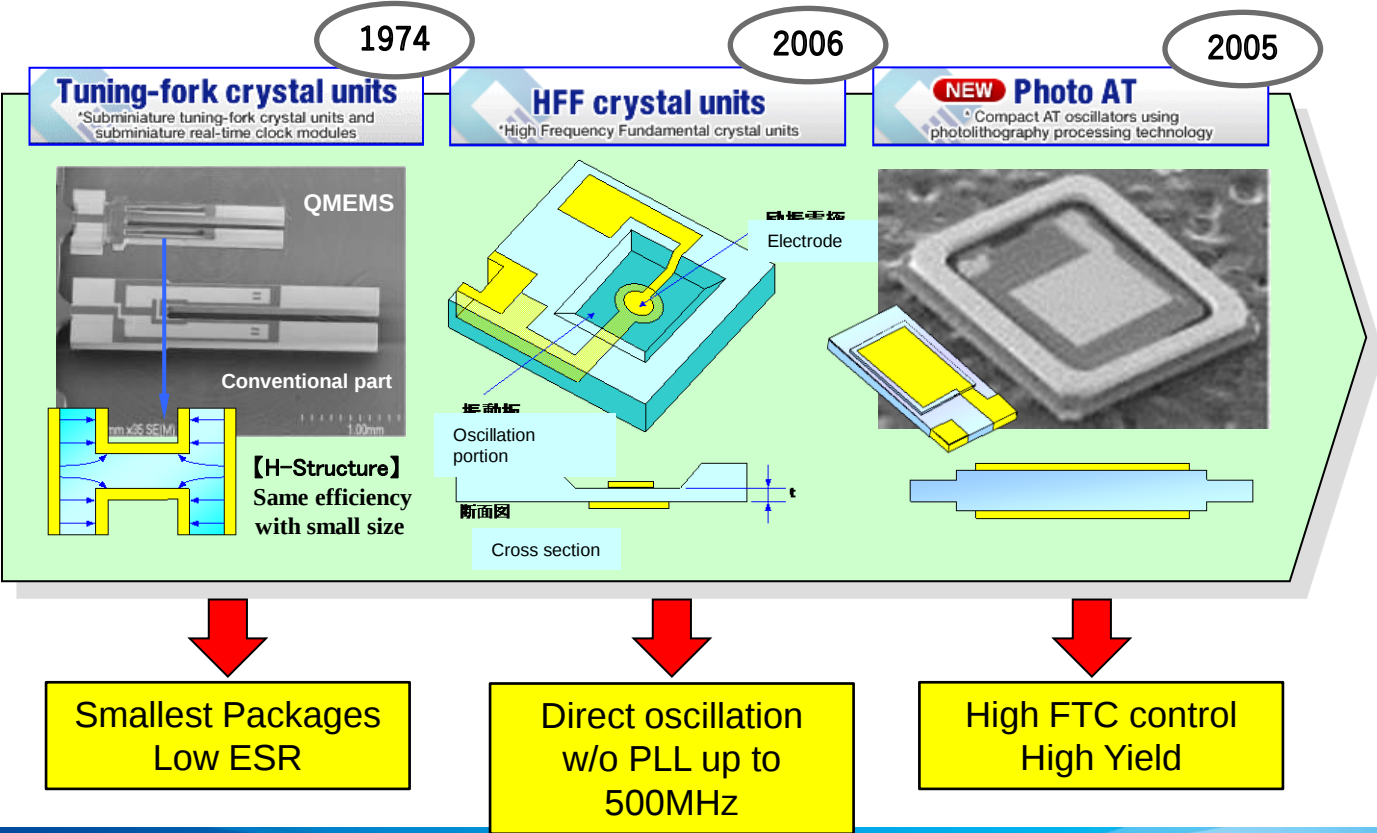
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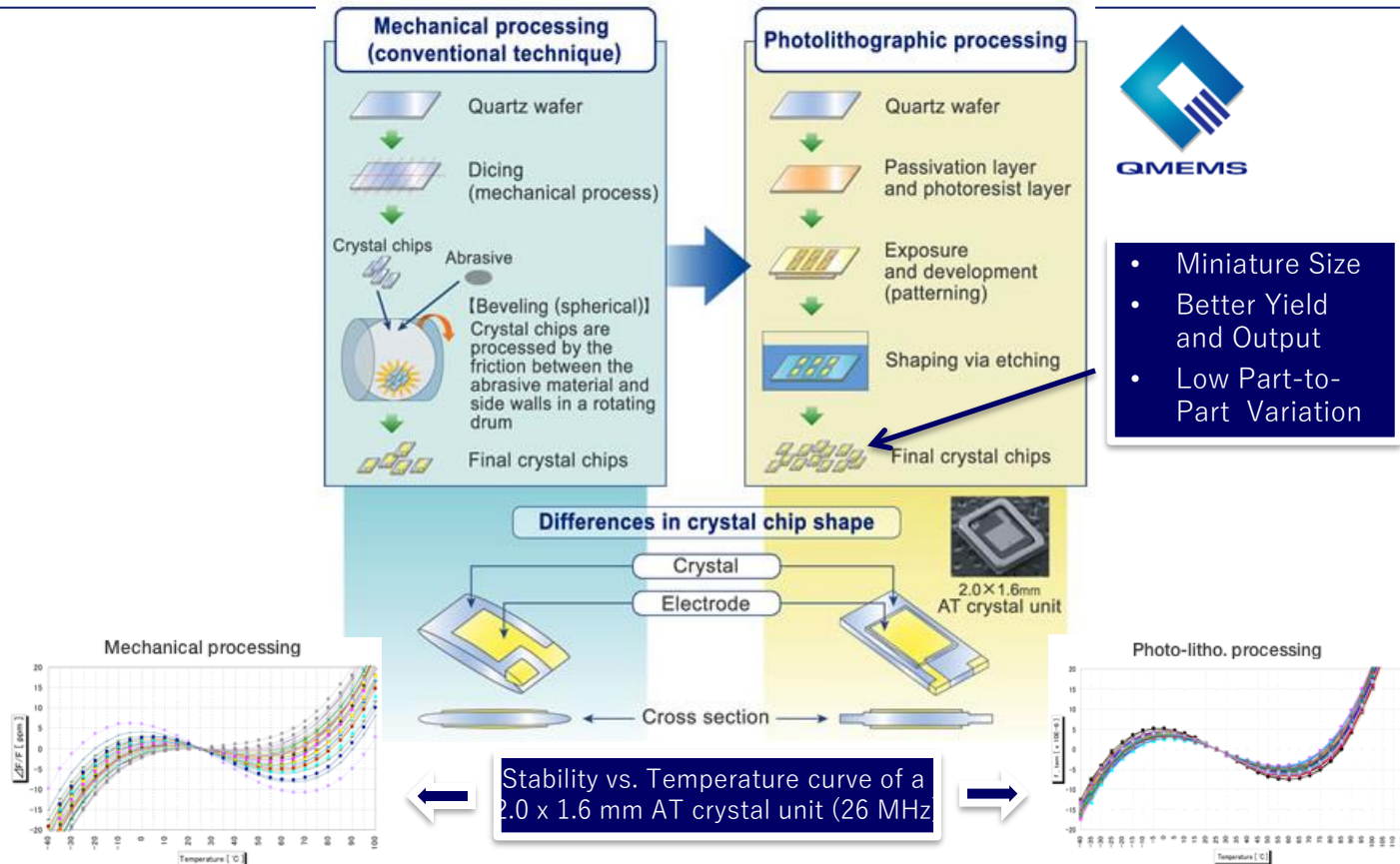
EXPLAINER VIDEO



Manufacturing Synthetic Quartz

QUARTZ+MEMS
high accuracy and high stability
Micro Electro
Mechanical Systems





Find out more here: <http://www5.epsondevice.com/en/quartz/aboutus/qmems/>

home



Production: Sakata
R&D: Fujimi

Advantages:

- Custom designs for timing
 - performance & features
- Cost
- Assurance of supply

Epson Timing IC IP:

- Oscillators
- Temperature compensation
- Integer and fractional PLLs
- AFEs for sensing

Epson ICs used in

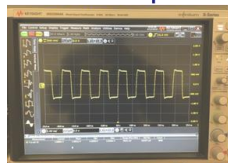
- RTCs
- SPXOs, SPSOs, & MOSOs
- VCXOs & VCSOs
- P-SPXOs & P-VCXOs
- TCXOs
- Gyros & IMUs

Altera Corporation • Circuit design • IC partners	ANALOG DEVICES • Circuit design • IC partners	Atmel • Circuit design • IC partners	Greenview Communications • IC partners
Inphi Corporation • IC partners	IDT • IC partners	ROHM GROUP LAPIS SEMICONDUCTOR • Circuit design • IC partners	Marvell Technology Group Ltd. • IC partners
Microchip Technology Inc. • IC partners	Microsemi Corporation • IC partners	NORDIC SEMICONDUCTOR • Circuit design • IC partners	MTT Electronics • IC partners
nuvoton • IC partners	NXP Semiconductors • Circuit design • IC partners	QLogic Corp. • IC partners	RENESAS • Circuit design • IC partners
ROHM • Circuit design • IC partners	SEMTECH • IC partners	SILICON LABS • IC partners	ST the augmented • Circuit design • IC partners
TEXAS INSTRUMENTS • Circuit design • IC partners	ublox • IC partners	Xilinx Inc. • Circuit design • IC partners	

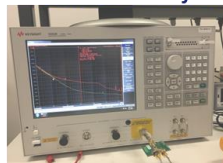
- Epson as leading manufacturer first choice at IC maker
- to approve 32KHz / MHz / TCXO for Wireless ICs
- to approve SPXO for FPGA and Networking
- > **safe design of oscillation circuit**
- > **quick definition of part number**
- > **high probability of sampling ex stock**
- > **Epson saves your time in the design phase !**



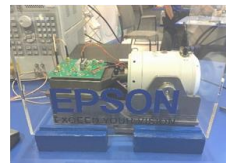
Oscilloscopes



Phase Noise Analyzer



Vibration Tester



GPS Time Reference



How to use the Index slide

EPSON

Jump to any product family you wish by clicking on any [hyperlink](#)

Click on [home](#) to return to the Product Line-up home page any time you like

Product Line-Up

- [kHz Crystal](#)
- [Real Time Clock Module](#)
- [MHz Crystal](#)
- [SPXO](#)
- [TCXO](#)
- [High end SPXO / TCXO / VCXO](#)
- [Clock Buffer](#)
- [Automotive Grade](#)



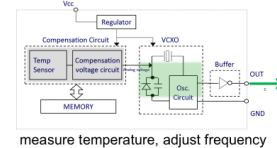
EPSON

TCXO Basics

EPSON

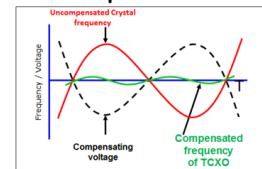
- Temperature
 - Compensated
 - X = Crystal
 - Oscillator
-
- **Important Specs**
 - Size
 - Frequency
 - Voltage
 - +/-2ppm or +/-0.5ppm Stability
 - Operating Temperature
 - Voltage Control
-
- **Key Applications**
 - GPS reference
 - RF reference

Basic Principle



measure temperature, adjust frequency

TCXO output: Green curve



Reference: John Vig's Tutorial

[home](#)

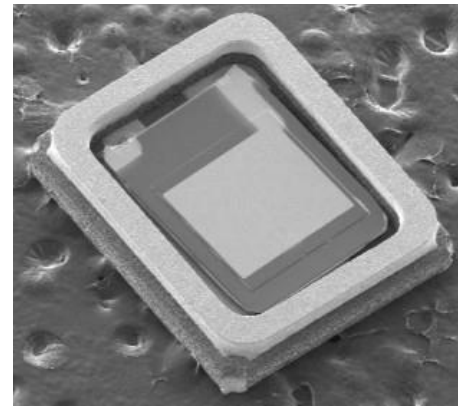
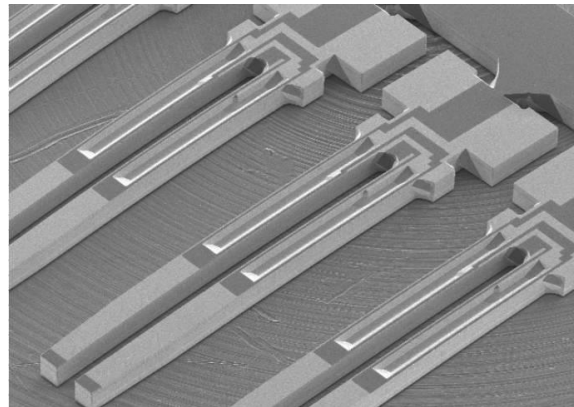


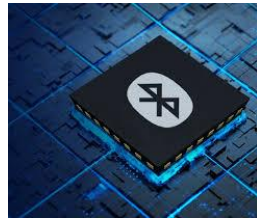
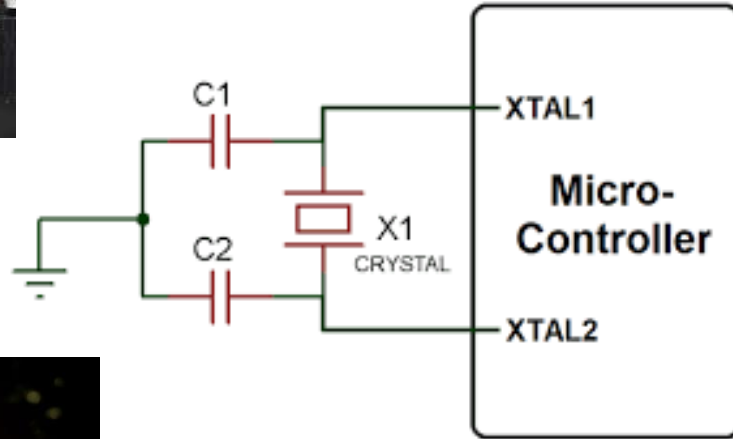
Timing Product Line-Up

- [kHz Crystal](#)
- [Real Time Clock Module](#)
- [MHz Crystal](#)
- [SPXO](#)
- [TCXO](#)
- [High-end clocks for Networking](#)
- [Clock Buffer](#) 
- [Automotive Grade](#) 

kHz and MHz Crystal

basic crystal elements for every application





Known As...

- Tuning Fork Crystal
- Clock Crystal

Important Specs

- Size
- Height
- Frequency Tolerance
- Load capacitance
- Equivalent Series Resistance (ESR)

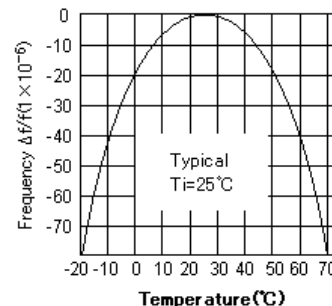
Key Applications

- MCU clocking
- Real Time Clock clocking



Flexural Vibration mode

kHz Frequency Deviation Temperature Curve

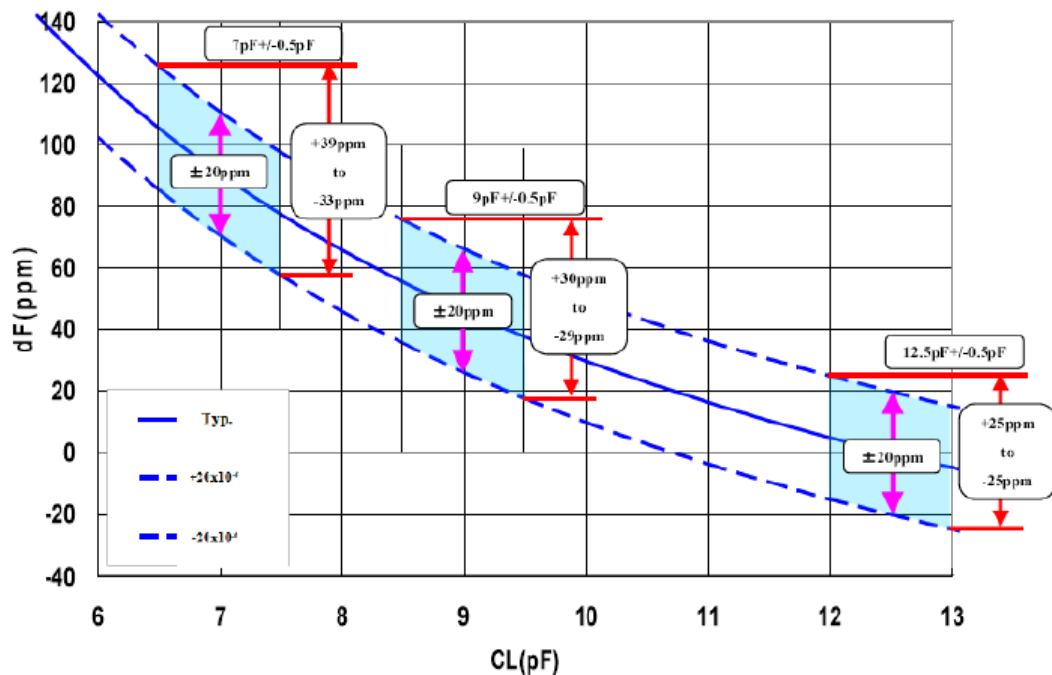


$$\Delta f/f = B(T_i - \theta X)^2$$

θX : specified temperature, B: Parabolic coefficient

Load Capacitance – the right choice

- ▶ Smaller Load Cap has the advantage of lower the current consumption at the oscillation circuit.
- ▶ On the others hand, smaller Load Cap makes the oscillation frequency unstable, design it difficult to improve time accuracy.



Oscillation circuit	CL value	Smaller	Larger
	R :Negative resistance	Larger	Smaller
	Oscillation allowance	Larger	Smaller
	Power consumption	Smaller	Larger
	Drive level	Smaller	Larger
	Frequency stability	Worse	Better
	Oscillation start-up time	Shorter	Longer

$$CL \cong \frac{CG \times CD}{CG + CD} + CS \text{ (Stray capacity)}$$

Low ESR for Low Power

▼ ES

▽ ES

In MP

In Design

Planned

Considering

Current Products

Crystal Unit

FC-135 / FC-135R

3.2 x 1.5 x 0.8t,
70 / 50 (R) kΩ,
Glass lid

FC-12M

2.0 x 1.2 x 0.6t, 90 kΩ, Metal lid

FC3215/2012AN

3.2 x 1.5 x 0.8t, 50 kΩ,
2.0 x 1.2 x 0.6t, 50 kΩ, Metal lid

FC1610AN

1.6 x 1.0 x 0.5t
90 kΩ,
Metal lid

FC2012SN

2.0 x 1.2 x 0.6t, 90 kΩ,
Metal lid

FC1610BN

1.6 x 1.0 x 0.5t
60 kΩ,
Metal lid

FC3215BN

3.2 x 1.5 x 0.8t
Same sensitivity as
FC-135R with PB-Free
Metal lid
ES: 3Q/'25, MP: 4Q/'25

CY25

1Q

2Q

3Q

4Q

CY26

1H

2H

CY27

1H

2H

CY28~

Low ESR and Miniature Size 32kHz XTAL

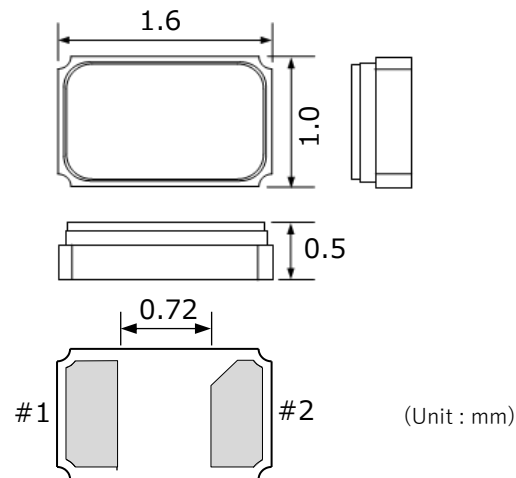
■ Feature

- Frequency range : 32.768 kHz
- Low ESR : 45 k Ω typ. at +25 °C
- Size : 1.65 x 1.05 x 0.5 t mm

■ Overview

Item	Symbol	Specifications	Conditions / Remarks
Nominal frequency range	f_nom	32.768 kHz	
Storage temperature	T_stg	-55 °C to +125 °C	Storage as single product.
Operating temperature	T_use	-40 °C to +105 °C	
Level of drive	DL	0.1 μ W (0.5 μ W Max.)	
Frequency tolerance	f_tol	$\pm 20 \times 10^{-6}$	+25 °C, DL=0.1 μ W
Turnover temperature	Ti	+25 °C ± 5 °C	
Parabolic coefficient	B	-0.04×10^{-6} / °C ² Max.	
Load capacitance	CL	9 pF, 12.5 pF	Please specify
Motional resistance (ESR)	R1	45 k Ω typ. at +25°C 60 k Ω Max. at -40 to +85 °C 70 k Ω Max. at -40 to +105 °C	
Motional capacitance	C1	7.5 fF typ.	
Shunt capacitance	C0	1.5 pF typ.	
Frequency aging	f_age	$\pm 3 \times 10^{-6}$ / year Max.	+25 °C, First year

■ External dimensions



■ Schedule
 ES : Done
 MP : 2Q/2024

home

Same Sensitivity as FC-135R with Pb Free

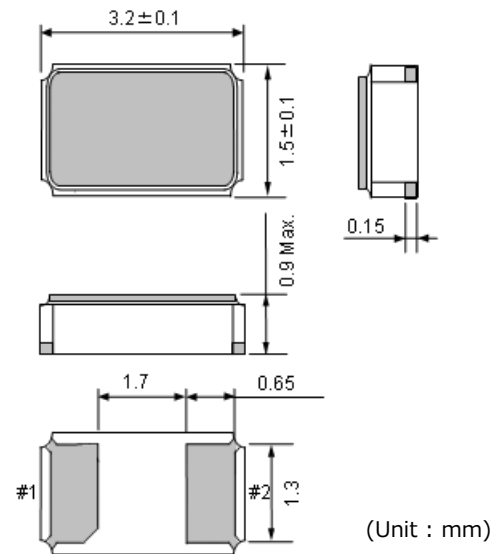
■ Feature

- Frequency range : 32.768 kHz
- Low ESR : 50 k Ω Max
- Size : 3.2 x 1.5 x 0.9 t mm
- Applications ; IoT devices, Modules, etc

■ Overview

Item	Symbol	Specifications	Conditions / Remarks
Nominal frequency range	f_nom	32.768 kHz	
Storage temperature	T_stg	-55 °C to +125 °C	Storage as single product.
Operating temperature	T_use	-40 °C to +105 °C	
Level of drive	DL	0.5 μ W (1.0 μ W Max.)	
Frequency tolerance	f_tol	$\pm 20 \times 10^{-6}$	+25 °C, DL=0.1 μ W
Turnover temperature	Ti	+25 °C ± 5 °C	
Parabolic coefficient	B	-0.04×10^{-6} / °C ² Max.	
Load capacitance	CL	7 pF, 9 pF, 12.5 pF	Please specify
Motional resistance (ESR)	R1	50 k Ω Max.	
Motional capacitance	C1	3.4 fF typ.	
Shunt capacitance	C0	1.0 pF typ.	
Frequency aging	f_age	$\pm 3 \times 10^{-6}$ / year Max.	+25 °C, First year

■ External dimensions



■ Schedule

ES : 2H/2024
MP : 1H/2025

High Stability Miniature Size 32k SPXO

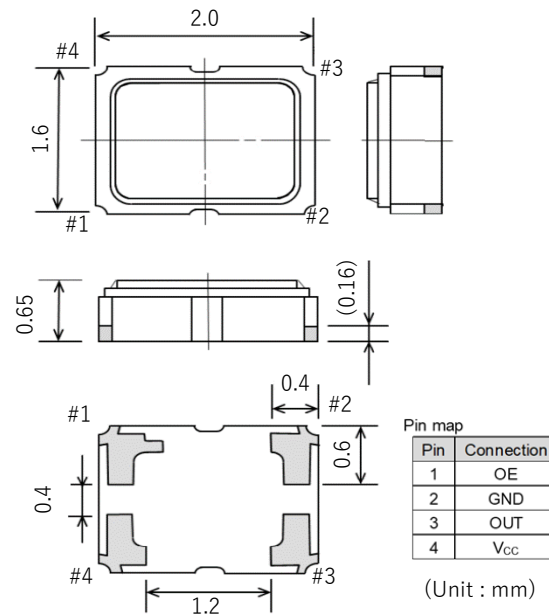
■ Features

- Output Frequency : 32.768kHz, CMOS output
- Low Current consumption : 0.4μA typ.
- Frequency Tolerance : $\pm 8.0 \times 10^{-6}$ (+25 °C)
- Size : 2.0 x 1.6 x 0.65t mm or 1.6 x 1.0 x 0.65t mm

■ Specifications

Item	Symbol	Specifications	Conditions / Remarks
Output frequency	f _o	32.768 kHz	
Supply voltage	V _{CC}	1.4 to 5.5 V	
Storage temperature	T _{stg}	-55 °C to +125 °C	Storage as single product.
Operating temperature	T _{use}	-40 °C to +105 °C	
Frequency / Temperature characteristics	F _{T_C}	$\pm 8.0 \times 10^{-6}$	T _a = 25 °C
Current consumption	I _{CC}	0.4μA typ.	No Load condition, V _{CC} = 1.8V
Symmetry	SYM	45 % to 55 %	50 % V _{CC} level
Output load condition (CMOS)	L _{CMOS}	30 pF Max.	
Start-up time	T _{str}	1 s Max.	T _a = +25 °C, V _{CC} = 1.5 V to 5.5 V
Cycle Jitter	t _{C-C}	5 ns Typ.	Please specify
Frequency aging	f _{age}	$\pm 3 \times 10^{-6}$ / year Max.	+25 °C, First year

■ External dimensions



■ Schedule
ES : TBD
MP: TBD

home

High Stability Miniature Size 32k TCXO

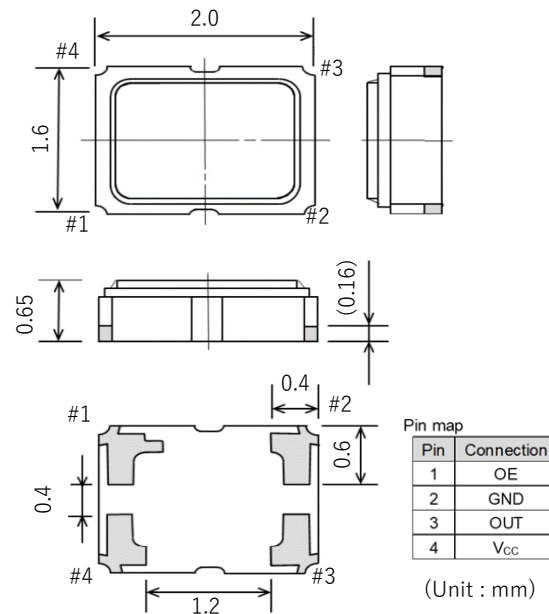
■ Features

- Output Frequency : 32.768kHz, CMOS output
- Low Current consumption : 0.5μA typ.
- Frequency Tolerance : $\pm 8.0 \times 10^{-6}$ (-40 °C to +105 °C)
- Size : 2.0 x 1.6 x 0.65t mm or 1.6 x 1.0 x 0.65t mm

■ Specifications

Item	Symbol	Specifications	Conditions / Remarks
Output frequency	f _o	32.768 kHz	
Supply voltage	V _{CC}	1.4 to 5.5 V	
Storage temperature	T _{stg}	-55 °C to +125 °C	Storage as single product.
Operating temperature	T _{use}	-40 °C to +105 °C	
Frequency / Temperature characteristics	F _{T_C}	$\pm 8.0 \times 10^{-6}$	T _a = -40 °C to +105 °C
Current consumption	I _{CC}	0.5μA typ.	No Load condition, V _{CC} = 1.8V
Symmetry	SYM	45 % to 55 %	50 % V _{CC} level
Output load condition (CMOS)	L _{CMOS}	30 pF Max.	
Start-up time	T _{str}	1 s Max.	T _a = +25 °C, V _{CC} = 1.5 V to 5.5 V
Cycle Jitter	t _{C-C}	5 ns Typ.	Please specify
Frequency aging	f _{age}	$\pm 3 \times 10^{-6}$ / year Max.	+25 °C, First year

■ External dimensions



■ Schedule
ES : TBD
MP: TBD

home

Known As...

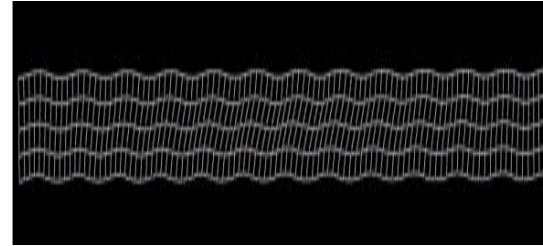
- AT Crystal
- RF Crystal

Important Specs

- Size
- Frequency
- Frequency Tolerance and Stability
- Operating Temperature
- Load Capacitance
- Equivalent Series Resistance (ESR)

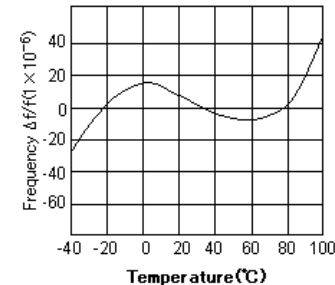
Key Applications

- Connectivity (WiFi, BT, Lora etc)
- RF Clocking
- MCU Clocking



Thickness Shear Vibration mode

MHz Frequency Deviation Temperature Curve



$$\Delta f/f = \alpha (\theta X - 25)^3 + \beta (\theta X - 25)^2 + \gamma (\theta X - 25)$$

θX : specified temperature

Miniaturization High Frequency/Tight Stability

▼ ES

▼ ES

In MP

In Design

Planned

Considering

Current Products

For Consumer/Industrial

FA-128

2.0 x 1.6 x 0.5t,
19.2 MHz to 54 MHz

FA-118T

1.6 x 1.2 x 0.35t,
24 MHz to 54 MHz
15 standard frequencies
(24/25/26/27/27.12/30/32/32.4/37.4/38.
4/39/40/48/50/52 MHz)

FA1210AN

1.2 x 1.0 x 0.3t,
32 MHz to 100 MHz
6 standard frequencies
(32/48/52/55.2/76.8/80 MHz
+ Planning: 40/153.6MHz)

FA1008AN

1.0 x 0.8 x 0.3t,
40 MHz to 100 MHz
5 standard frequencies
(48/52/59.97/76.8/80 MHz
+ Planning: 32/40/153.6MHz)

CY25

1Q

2Q

3Q

4Q

Jan

Apr

Jul

Oct

Updated Operating Temperature
range

Original : -40 to 105 °C
New: -40 to 125 °C

CY26

1Q

2Q

3Q

4Q

FA-118T
FA1210AN
FA1008AN

Tight stability Ver.

Total $\pm 20 \times 10^{-6}$ for -40 to 105 °C

Total $\pm 20 \times 10^{-6}$ for -40 to 85 °C

ES: Q2/CY26, MP: Q4/CY26

CY27

1H

2H

CY28~

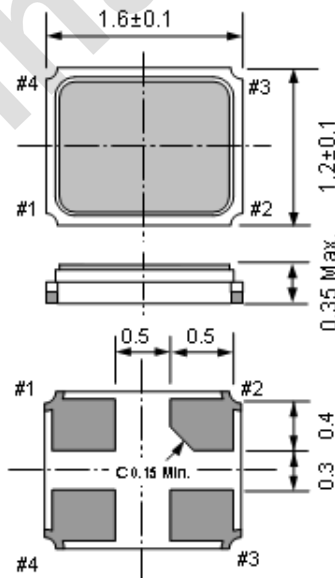
■ Features

- Ultra Small size with low height package crystal unit.
1.6 × 1.2 mm, t = 0.35 mm Max.
- Best for small size application such as...
Small wireless device, Small wireless module, and Wearable device, etc

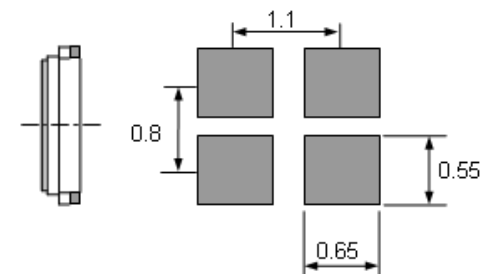
■ Specifications

Item	Specifications
Nominal frequency range	52 to 80 MHz
Storage temperature range	-40 °C to +125 °C
Operating temperature range	-40 °C to +105 °C
Level of drive	200 μ W Max.
Frequency tolerance	$\pm 7 \times 10^{-6}$
Load capacitance	6 pF to ∞
Motional resistance (ESR)	60 Ω Max.
Frequency versus temperature characteristics.	$\pm 10 \times 10^{-6}$ / -30 °C to +85 °C
Frequency Aging (5 years at +25 °C) Reflow shift (After 2 reflows)	$\pm 3 \times 10^{-6}$

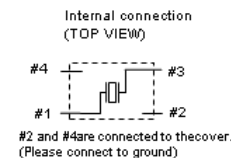
■ External dimension



■ Footprint



■ Schedule
ES : 4Q/'25
MP : 2Q/'26



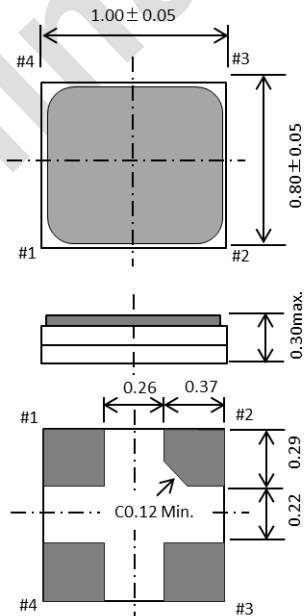
■ Features

- Ultra Small size with low height package crystal unit.
1.0 × 0.8 mm, t = 0.3 mm Max.
- Best for small size application such as...
Small wireless device, Small wireless module, and Wearable device, etc

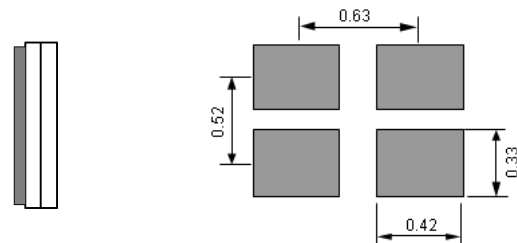
■ Specifications

Item	Specifications
Nominal frequency range	52 to 80 MHz
Storage temperature range	-40 °C to +125 °C
Operating temperature range	-40 °C to +105 °C
Level of drive	200 μ W Max.
Frequency tolerance	$\pm 7 \times 10^{-6}$
Load capacitance	6 pF to ∞
Motional resistance (ESR)	60 Ω Max.
Frequency versus temperature characteristics.	$\pm 10 \times 10^{-6}$ / -30 °C to +85 °C
Frequency Aging (5 years at +25 °C) Reflow shift (After 2 reflows)	$\pm 3 \times 10^{-6}$

■ External dimension



■ Footprint



Internal connection
(TOP VIEW)

#2 and #4 are connected to the cover.
Please connect to ground

■ Schedule
ES : 4Q/'25
MP : 2Q/'26

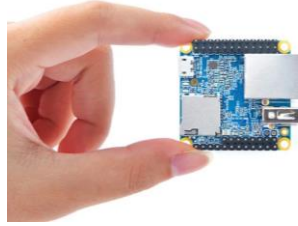
RTC Module

Integrated Module with 32KHz crystal & Epson IC

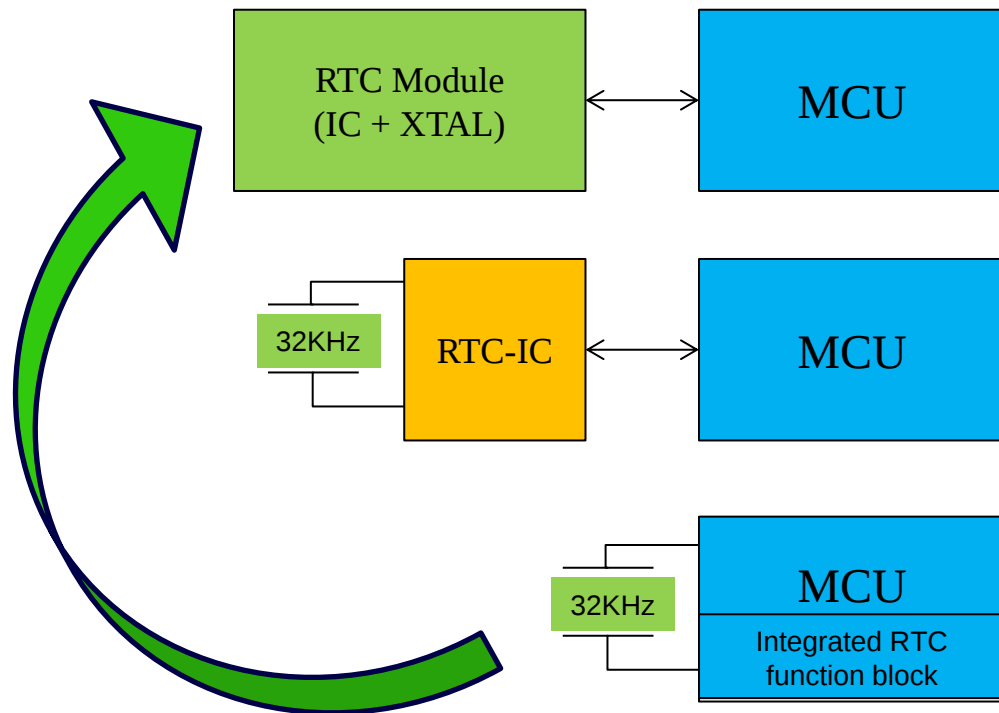


Applications for RTC Modules

EPSON



home

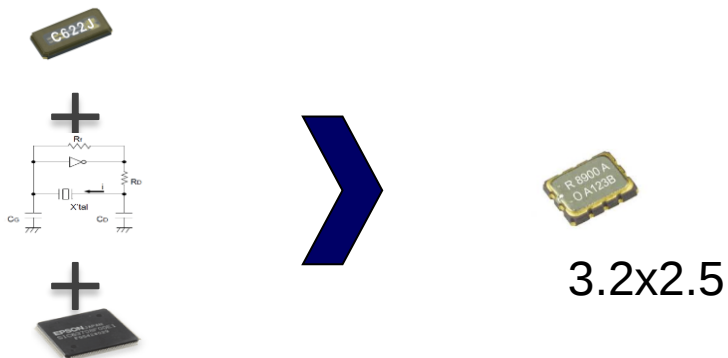


up-grade your application !

low power
high accuracy
optional power switch
battery charge control
event detection
one package: reliable & tiny
overall cost

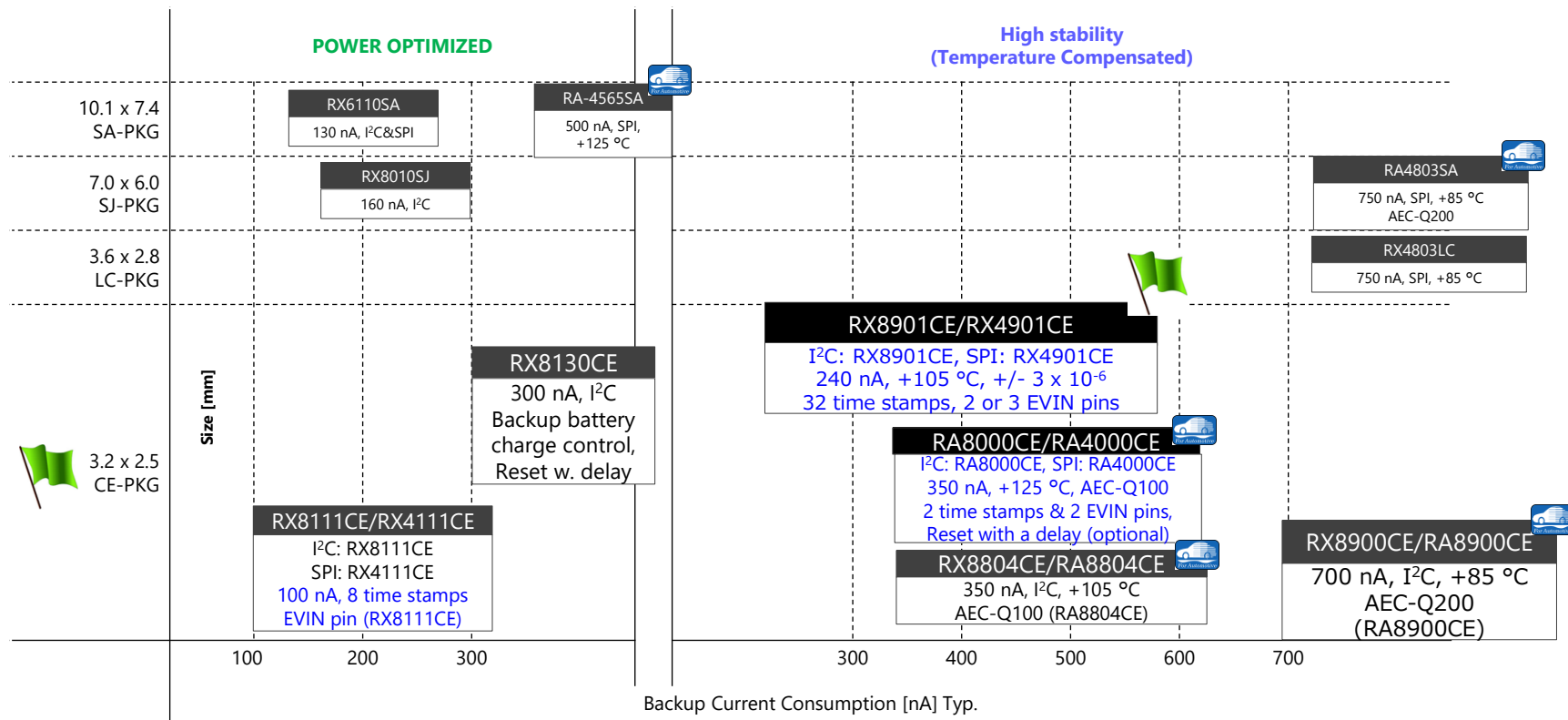
low power
optional power switch
battery charge control

lowest *component* cost
power consumption ?
stability / calibration ?
oscillator circuit design ?
additional functions ?
reliability ?
overall cost inc production ?



KHz + MCU	RTC Module
32KHz discrete needed	32KHz integrated
proper 32KHz osc design	included
calibration needed	included and optimized
power switch needed	included and optimized
battery size & service time	optimized power consumption
time stamps	included and optimized

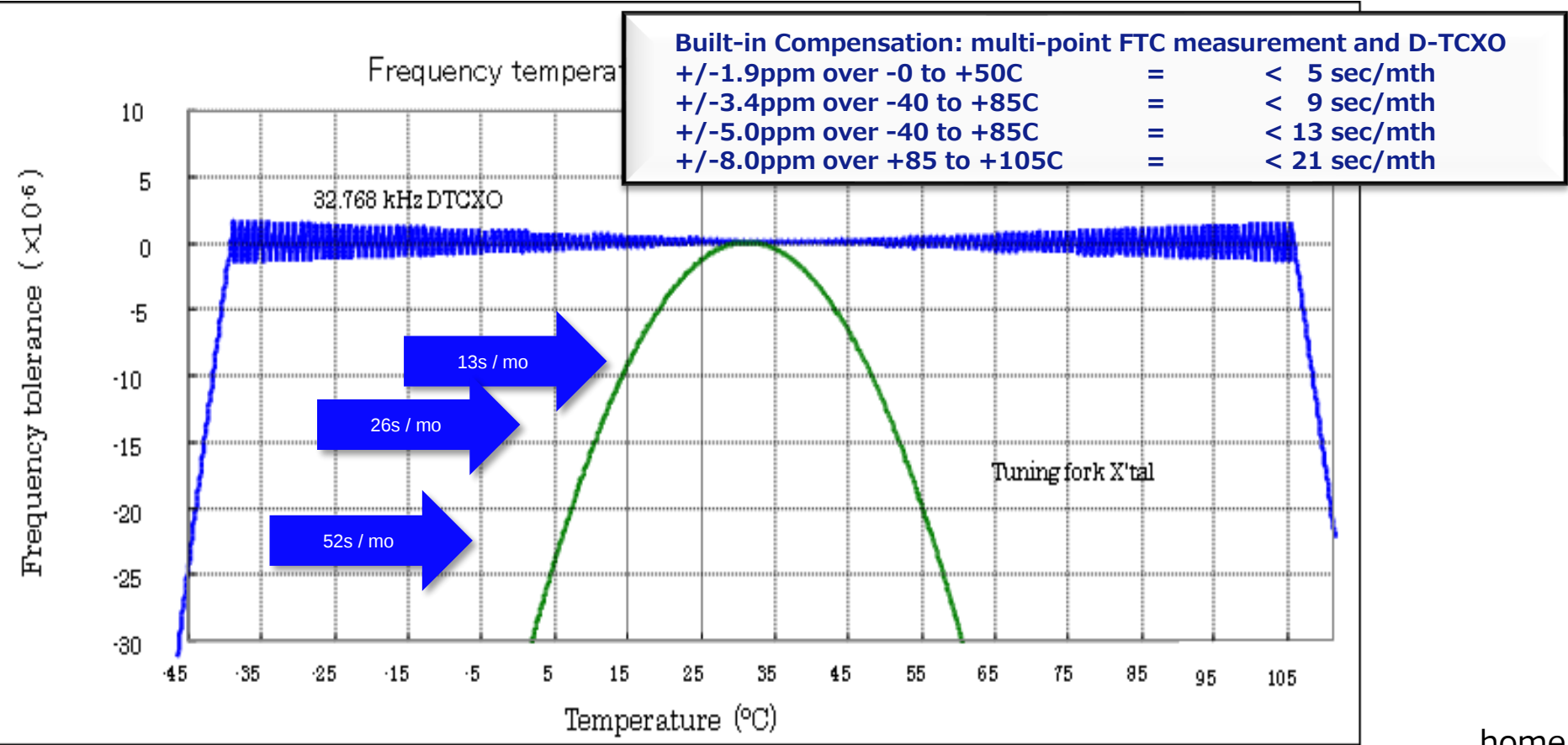
Real Time Clock module

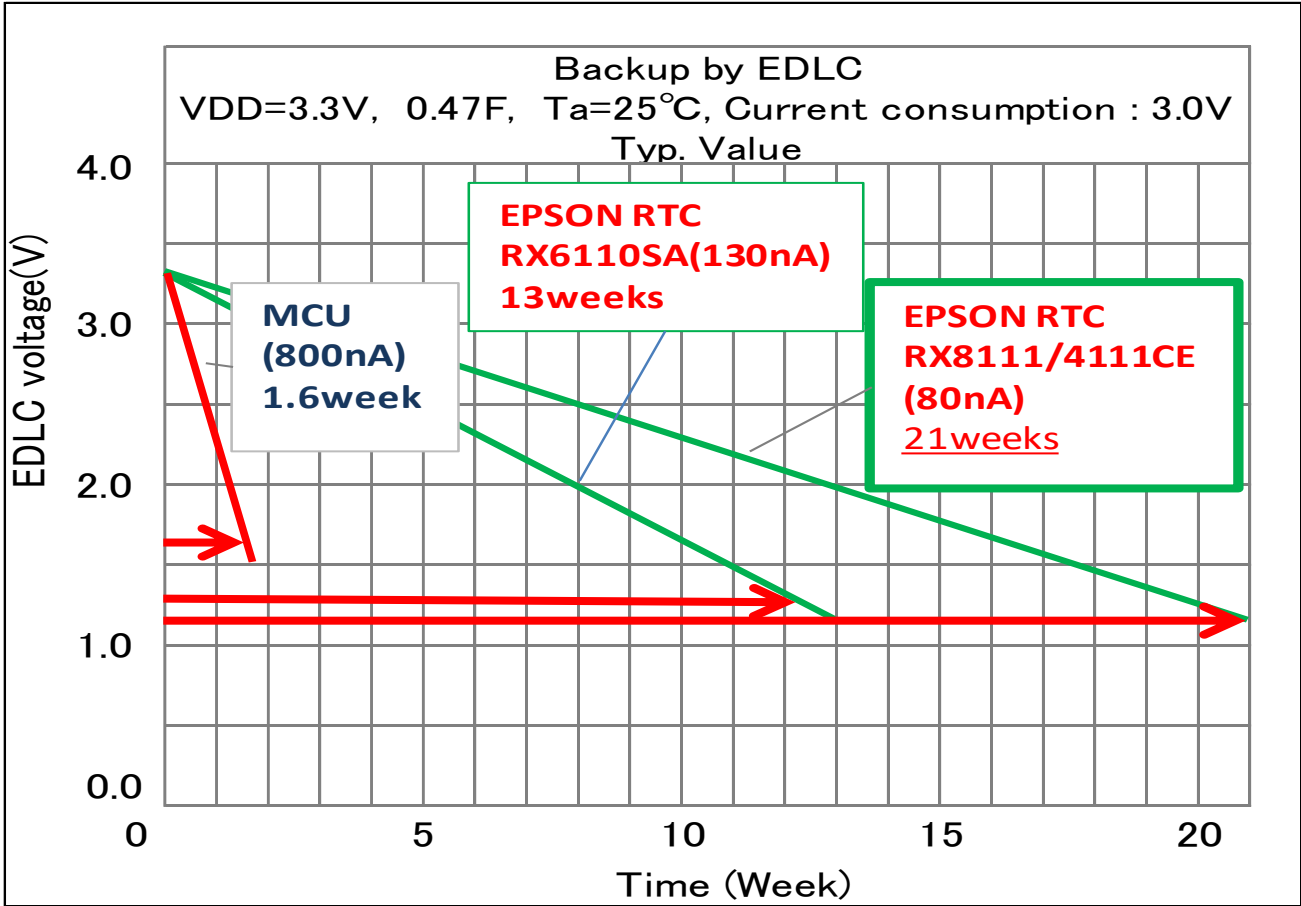


Comparison 3.2x2.5 size

	RX8111CE	RX4111CE	RX8130CE	RX8804CE	RX8900CE	RX8901CE
DTCXO				Built-in	Built-in	Built-in
Interface	I ² C	SPI	I ² C	I ² C	I ² C	I ² C
Up to +105 °C				Yes		Yes
Backup current Typ. / 3 V	100 nA	100 nA	300 nA	350 nA	700 nA	250 nA
Time stamp	Yes, 8 times	Yes, 8 times		Yes, 1 time		Yes, 32 times
EVIN pin	Yes			Yes		Yes, 3
Power switching	Yes	Yes *Need external Diode for V _{BAT}	Yes, Built-in backup battery charge control function		Yes *Need external Diode for V _{BAT}	Yes
Reset output			Yes			
Pricing	\$\$	\$\$	\$	\$\$\$	\$\$\$	\$\$\$

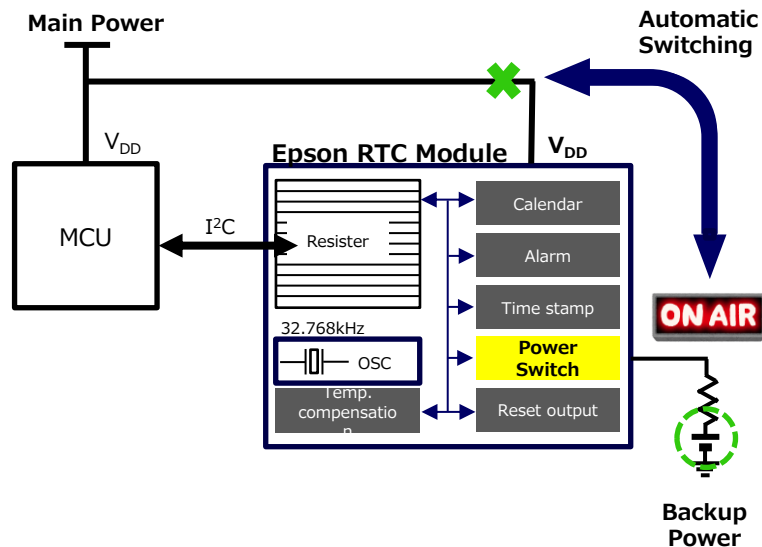
High Stability over Temperature Range





Minimum
clock Voltage

This monitors the main power condition, and this will automatically change the power source to backup mode when the voltage on the main power drops.



Advantages vs Diode-OR circuit

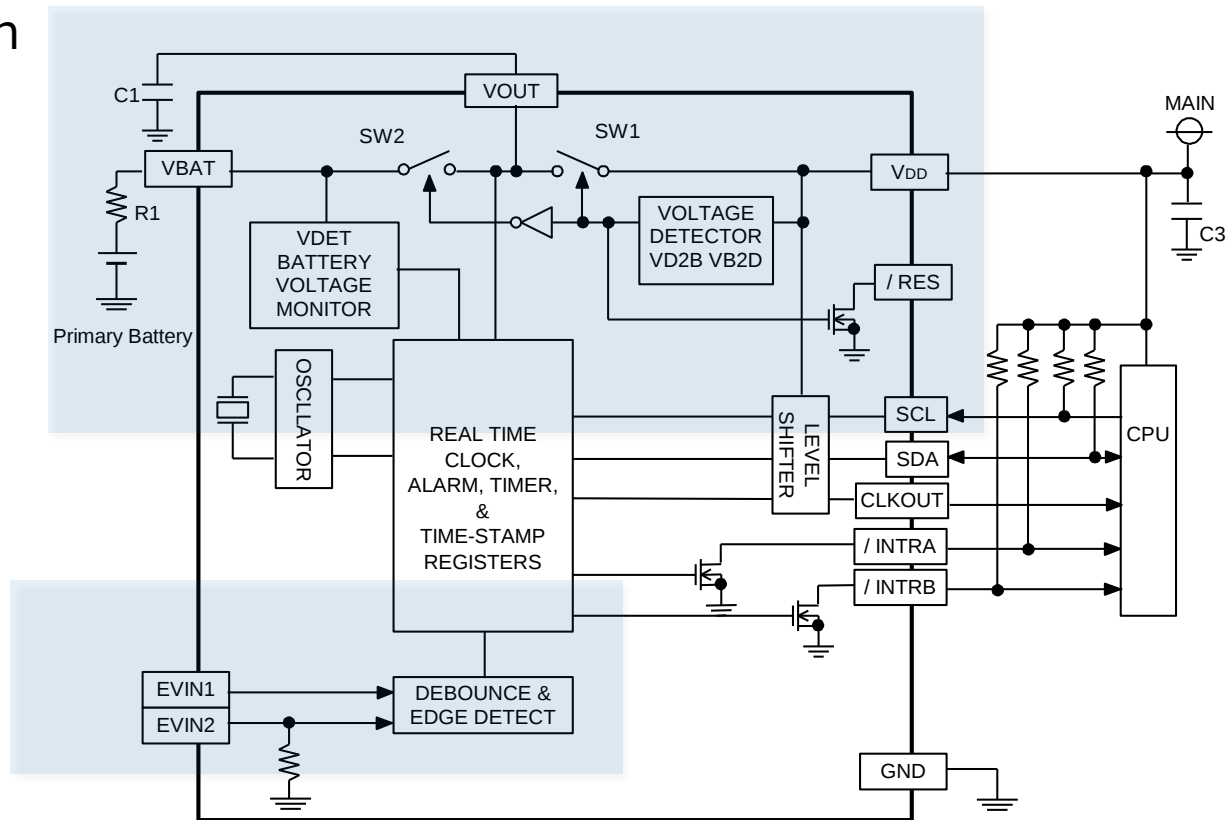
- Reduce a leak current

By using MOS switch in RTC module, user doesn't care about VF/IR specification of Diode.

*Depends on backup battery type

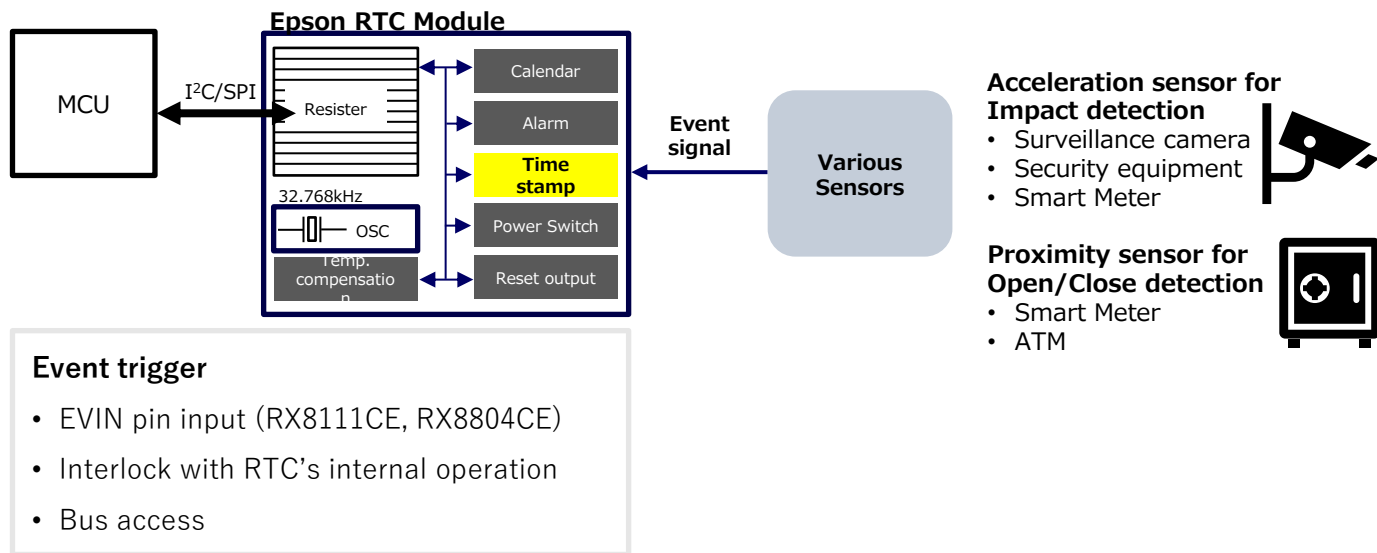
Battery Switch

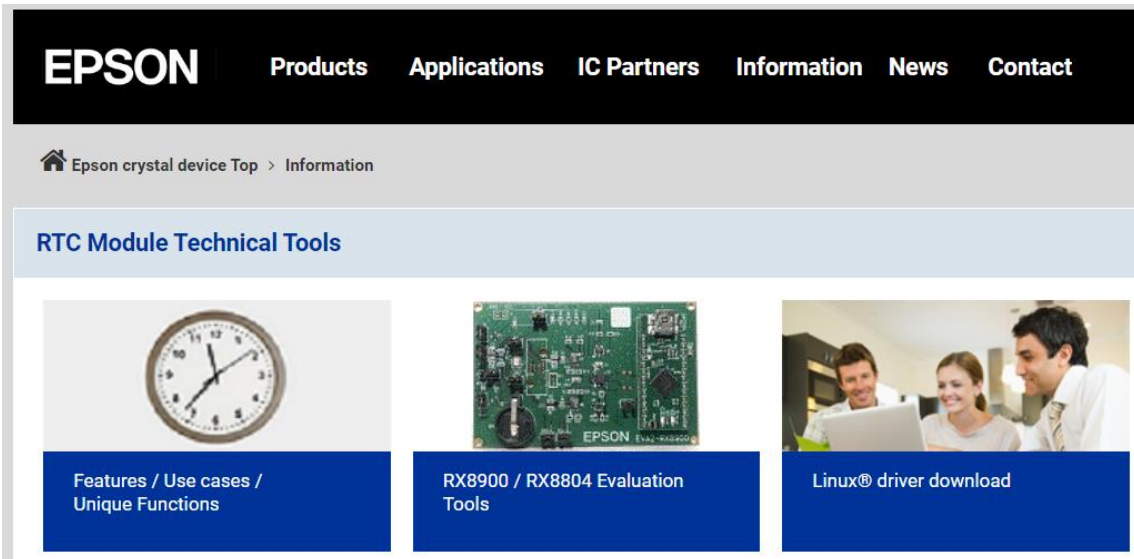
Event Detection



This function records the time data when an event (signal) is detected.

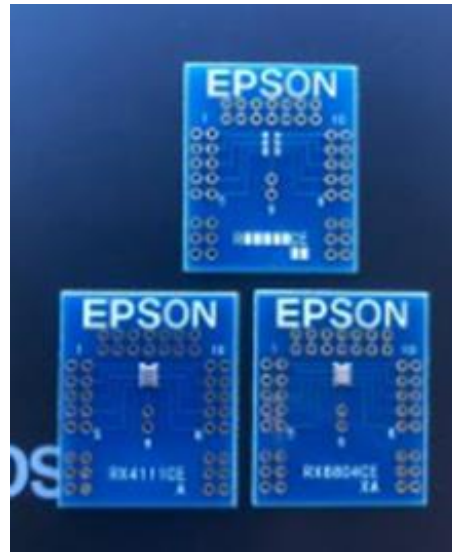
- RX8111CE and RX8804CE can receive event signals directly from the event input pin (EVIN), enabling RTC operation even when the MCU is in standby mode.
- RX8111CE and RX4111CE can record 8 times clock time data. (User can select first/last 8times)





<https://www5.epsondevice.com/en/information/>

Extensive information on the RTC portfolio including application manuals and Linux drivers



Possibility to offer RTC Adapter-boards for evaluation purposes.

! Get in direct contact with Epson for online support

home

SPXO

CMOS Standard Oscillators with Epson IC inside





Basic Principle

- Crystal + amplifier IC Packaged Together
- No need for circuit evaluation

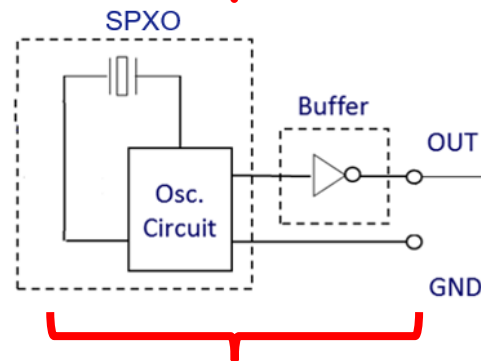
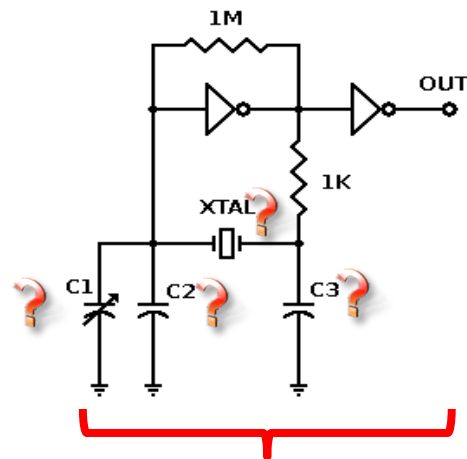
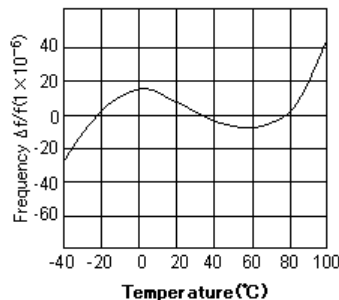
Important Specs

- Phase Noise / Jitter
- Package Size
- Stability

Key Applications

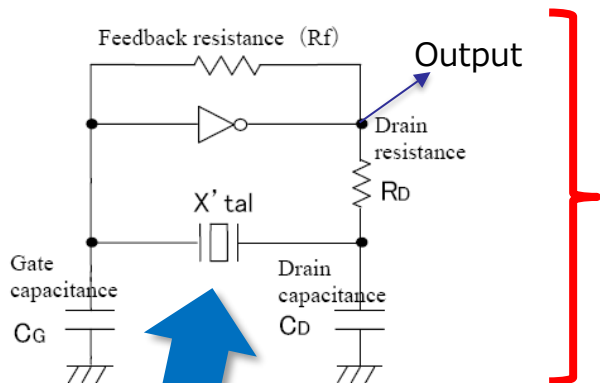
- Medical
- Networking
- Test and Measurement
- Industrial Automation

Frequency Tolerance “S” curve



Crystal

Typical Pierce Oscillator Circuit

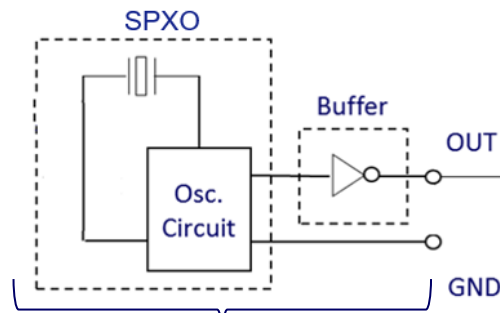


PCB Area Required



Small Crystal 1.6x1.2mm + External Components
Load Caps & Resistors

Oscillator



PCB Area Required



Small SPXO
2.0x1.6mm

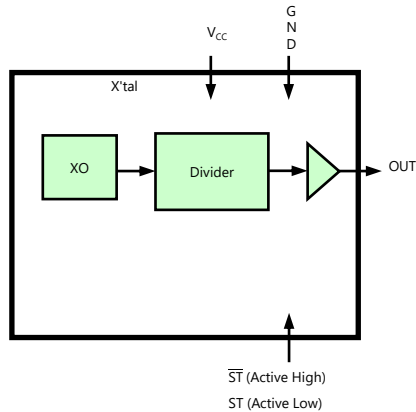
Direct „fixed frequency“ SPXO

20 standard frequencies

4/8/10/12/12.288/14.7456/16/20/24/24.675/25/26/27
/32/33.33/33.3333/40/48/50/72MHz

SG7050/5032/3225/2016

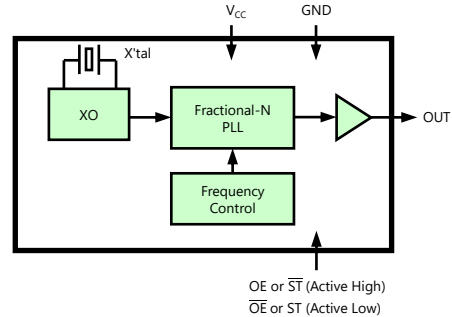
SG-210STF



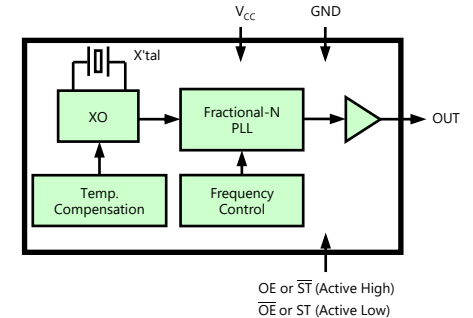
PLL „programmable“ SPXO

All non-standard frequencies

SG8018xx/SG8200xx



SG8101xx/ SG8201xx



SPXO – CMOS output

EPSON

ES

ES

In MP

In Design

Planned

Considering

Current Products

CY24

1Q

2Q

3Q

4Q

CY25

1Q

2Q

3Q

4Q

CY26

1H

2H

CY27~

SPXO (Standard Frequency)

SG-210STF SG-2016/3225/5032/7050CAN

SG-210STF: 2.5 x 2.0 x 0.8t
Others: 2.0 x 1.6 x 0.7t / 3.2 x 2.5 x 1.05t
/ 5.0 x 3.2 x 1.1t / 7.0 x 5.0 x 1.3t
1.5 MHz to 75 MHz, Jitter 0.3 ps Typ.
 $\pm 50 \times 10^{-6}$ (-40 to +105 °C)

Programmable SPXO

SG-8101/8018CG/CE/CB/CA

CG: 2.5 x 2.0 x 0.7t / CE: 3.2 x 2.5 x 1.05t / CB: 5.0 x 3.2 x 1.1t / CA: 7.0 x 5.0 x 1.3t
0.67 MHz to 170 MHz, Jitter 50 ps Typ.
SG-8101Cx: $\pm 15 \times 10^{-6}$ (-40 °C to +85 °C)
 $\pm 20 \times 10^{-6}$ (-40 °C to +105 °C)
Includes first year aging
SG-8018Cx: $\pm 50 \times 10^{-6}$ (-40 °C to +105 °C)
Includes 10 years aging

SG-9101CG/CE/CB/CA

CG: 2.5 x 2.0 x 0.7t / CE: 3.2 x 2.5 x 1.05t / CB: 5.0 x 3.2 x 1.1t / CA: 7.0 x 5.0 x 1.3t
0.67 MHz to 170 MHz,
Spread spectrum,
 $\pm 15 \times 10^{-6}$ (-40 °C to +85 °C)
 $\pm 20 \times 10^{-6}$ (-40 °C to +105 °C)
Includes first year aging

SG-8201/8200CJ/CG

CJ: 2.0 x 1.6 x 0.6t / CG: 2.5 x 2.0 x 0.7t
1.2 MHz to 170 MHz, Jitter 1.2 ps Typ.
SG-8201Cx: $\pm 15 \times 10^{-6}$ (-40 °C to +105 °C)
 $\pm 25 \times 10^{-6}$ (-40 °C to +125 °C)
Includes first year aging
SG-8200Cx: $\pm 50 \times 10^{-6}$ (-40 °C to +125 °C)
Includes first year aging

SG1612CRN

1.6 x 1.2 x 0.55t Max., ST function
4/20/24/25/26/27/40/
48/50/74.25 MHz
Jitter 0.2 ps Typ.
 $\pm 15 \times 10^{-6}$ (-40 °C to +105 °C)
ES: '25/1Q, MP: '25/2Q

SG2520CRN

2.5 x 2.0 x 0.7t, ST function
2.5 MHz to 80 MHz
Jitter 0.2 ps Typ.
 $\pm 15 \times 10^{-6}$ (-40 °C to +105 °C)
ES: TBD, MP: TBD

SG1210CRN

1.2 x 1.0 x 0.5t Max., ST function
4/20/24/25/26/27/40/
48/50/74.25 MHz
Jitter 0.2 ps Typ.
 $\pm 15 \times 10^{-6}$ (-40 °C to +105 °C)
ES: TBD, MP: TBD

SG2016CRN

2.0 x 1.6 x 0.6t, ST function
2.5 MHz to 80 MHz
Jitter 0.2 ps Typ.
 $\pm 15 \times 10^{-6}$ (-40 °C to +105 °C)
ES: TBD, MP: TBD

SG2520CBN

2.5 x 2.0 x 0.7t
76.8/98.304/100/125/
150/156.25 MHz
Jitter 0.6 ps Max.
 $\pm 15 \times 10^{-6}$ (-40 °C to +105 °C)
 $\pm 25 \times 10^{-6}$ (-40 °C to +125 °C)
 $\pm 50 \times 10^{-6}$ (-40 °C to +125 °C) Includes
first year aging

SG2016CBN

2.0 x 1.6 x 0.6t
76.8/98.304/100/125/
150/156.25 MHz
Jitter 0.6 ps Max.
 $\pm 15 \times 10^{-6}$ (-40 °C to +105 °C)
 $\pm 25 \times 10^{-6}$ (-40 °C to +125 °C)
 $\pm 50 \times 10^{-6}$ (-40 °C to +125 °C) Includes
first year aging

Jan

Apr

Jul

Oct

home

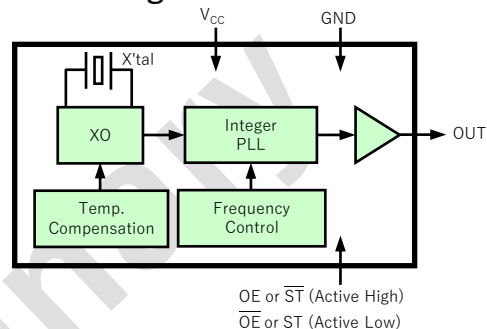
Feature

- Low noise Integer PLL technology support
- Jitter characteristics **0.6 ps Max.** at $f_0 = 125$ MHz
- $\pm 15 \times 10^{-6}$ (up to $+105^\circ\text{C}$) / $\pm 25 \times 10^{-6}$ (up to $+125^\circ\text{C}$) with Temperature compensation function

Specifications

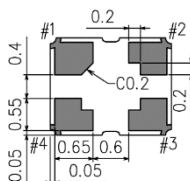
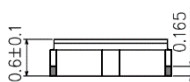
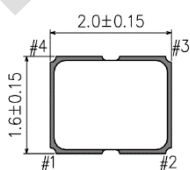
Item	Specifications
Standard frequency (f_0)	76.8 MHz / 98.304 MHz / 100 MHz 125 MHz / 150 MHz / 156.25 MHz
Output	CMOS
Supply voltage (V_{CC})	1.62 V to 3.63 V
Frequency tolerance / Operating temperature	$\pm 15 \times 10^{-6}$ / -40°C to $+105^\circ\text{C}$ $\pm 25 \times 10^{-6}$ / -40°C to $+125^\circ\text{C}$ $\pm 50 \times 10^{-6}$ / -40°C to $+125^\circ\text{C}$ * Including includes Initial frequency tolerance, Frequency / temperature characteristics, Frequency / voltage coefficient, Frequency / load coefficient and Aging (+25 °C, First year)
Current consumption (No load)	11.6 mA Max. ($f_0 \leq 100$ MHz) 13.2 mA Max. ($100 \text{ MHz} < f_0 \leq 125$ MHz) 16.6 mA Max. ($f_0 > 125$ MHz)
Symmetry	45 % to 55 %
Rise/Fall time	2.5 ns Max. ($f_0 \leq 125$ MHz) 2.0 ns Max. ($f_0 > 125$ MHz)
Phase jitter (@125 MHz)	0.6 ps Max. / 12 kHz to 20 MHz
Function	Output enable or Stand-by

Block diagram

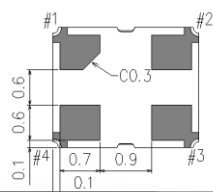
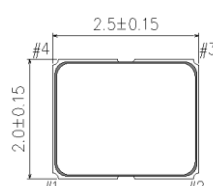


External dimension (unit in mm)

< SG2016CBN >



< SG2520CBN >



Schedule

SG2016CBN: ES: Done
MP: 7/CY24
SG2520CBN: ES: Done
MP: 7/CY24

Pin map

#1	OE or $\overline{\text{ST}}$ (Active High) ST or $\overline{\text{OE}}$ (Active Low)
#2	GND
#3	OUT
#4	Vcc

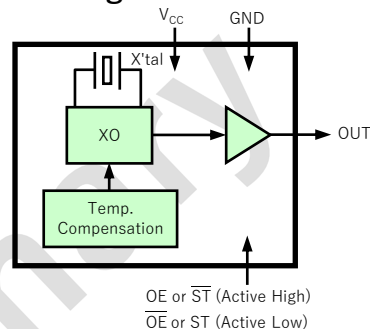
Feature

- High frequency stability in up to +105 ° C
- Tight symmetry
- Precise and Low phase noise

Specifications

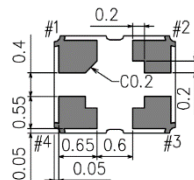
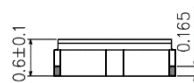
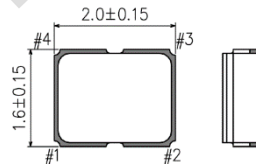
Item	Specifications
Frequency (fo)	10 MHz to 80 MHz
Output	CMOS
Supply voltage (V _{CC})	1.8 V ± 5 % / 2.5 V ± 10 % / 3.3 V ± 10 %
Frequency tolerance / Operating temperature	± 15 x 10 ⁻⁶ / -40 ° C to +105 ° C * Including includes Initial frequency tolerance, Frequency / temperature characteristics, Frequency / voltage coefficient, Frequency / load coefficient, and Aging (+25 ° C, First year)
Current consumption (@26 MHz, No load)	3.5 mA Max.
Symmetry	45 % to 55 % (opt. 49 % to 51 %)
Phase noise (@26 MHz)	-148 dBc/Hz Typ. at 1 kHz -169 dBc/Hz Typ. at 100 kHz
Phase jitter (@26 MHz)	0.2 ps Typ. / 12 kHz to 20 MHz
Function	Output enable or Stand-by

Block diagram

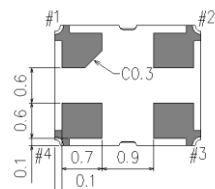
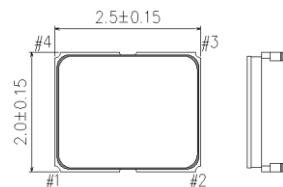


External dimension (unit in mm)

< SG2016CRN >



< SG2520CRN >



Schedule

SG2016CRN: ES: TBD
MP: TBD
SG2520CRN: ES: TBD
MP: TBD

Pin map

#1	OE or $\overline{ST}$ (Active High) ST or $\overline{OE}$ (Active Low)
#2	GND
#3	OUT
#4	V _{CC}

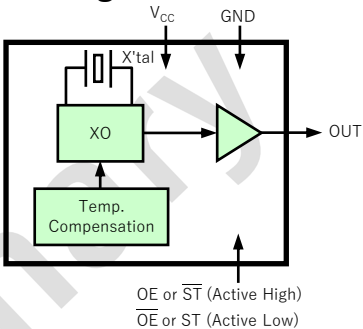
Feature

- High frequency stability in up to +105 ° C
- Tight symmetry
- Precise and Low phase noise

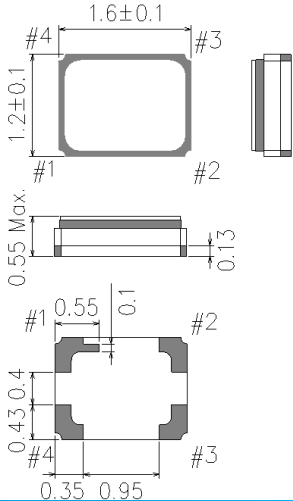
Specifications

Item	Specifications
Frequency (fo)	10 MHz to 80 MHz
Output	CMOS
Supply voltage (Vcc)	1.8 V ± 5 % / 2.5 V ± 10 % / 3.3 V ± 10 %
Frequency tolerance / Operating temperature	± 15 x 10 ⁻⁶ / -40 ° C to +105 ° C * Including includes Initial frequency tolerance, Frequency / temperature characteristics, Frequency / voltage coefficient, Frequency / load coefficient, and Aging (+25 ° C, First year)
Current consumption (@26 MHz, No load)	3.5 mA Max.
Symmetry	45 % to 55 % (opt. 49 % to 51 %)
Phase noise (@26 MHz)	-145 dBc/Hz Typ. at 1 kHz -159 dBc/Hz Typ. at 100 kHz
Phase jitter (@26 MHz)	0.2 ps Typ. / 12 kHz to 20 MHz
Function	Output enable or Stand-by

Block diagram



External dimension (unit in mm)



Schedule

ES: 1Q/CY25
MP: 2Q/CY25

Pin map

#1	OE or $\overline{ST}$ (Active High) ST or $\overline{OE}$ (Active Low)
#2	GND
#3	OUT
#4	Vcc

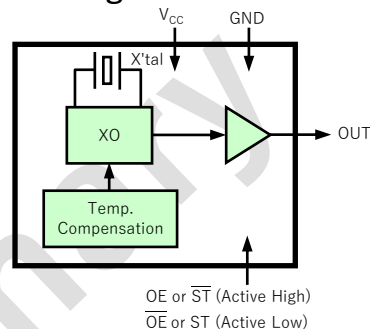
Feature

- High frequency stability in up to +105 ° C
- Tight symmetry
- Precise and Low phase noise

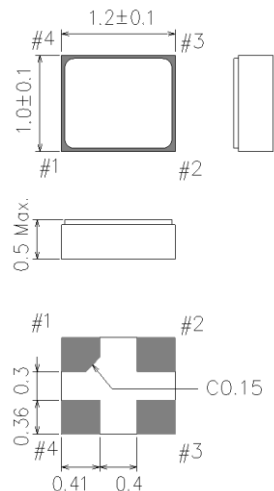
Specifications

Item	Specifications
Frequency (fo)	10 MHz to 80 MHz
Output	CMOS
Supply voltage (V _{CC})	1.8 V ± 5 % / 2.5 V ± 10 % / 3.3 V ± 10 %
Frequency tolerance / Operating temperature	± 15 x 10 ⁻⁶ / -40 ° C to +105 ° C * Including includes Initial frequency tolerance, Frequency / temperature characteristics, Frequency / voltage coefficient, Frequency / load coefficient, and Aging (+25 ° C, First year)
Current consumption (@26 MHz, No load)	3.5 mA Max.
Symmetry	45 % to 55 % (opt. 49 % to 51 %)
Phase noise (@26 MHz)	-145 dBc/Hz Typ. at 1 kHz -159 dBc/Hz Typ. at 100 kHz
Phase jitter (@26 MHz)	0.2 ps Typ. / 12 kHz to 20 MHz
Function	Output enable or Stand-by

Block diagram



External dimension (unit in mm)



Schedule

ES: TBD
MP: TBD

Pin map

#1	OE or ST (Active High) ST or OE (Active Low)
#2	GND
#3	OUT
#4	Vcc

Programmable
Simple
Packaged
X = Crystal
Oscillator

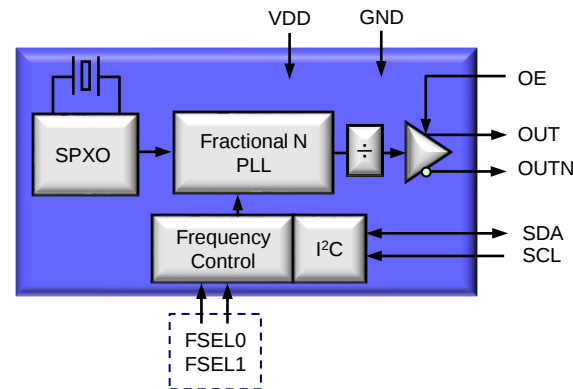
Important Specs

- Frequency
- Tolerance
- Operating Temperature
- Phase Noise/Jitter

Key Applications

- Medical
- Networking
- Test & Measurements
- Industrial Automation

Programmable oscillator using Fractional-N PLL to synthesis any frequency.



Basic Building Blocks:

1. Oscillator: SPXO
2. Fractional-N PLL
3. Output Buffer & Divider: CMOS or LVPECL
4. Control Block
 1. Select Pins
 2. I2C Interface1

Programmable SPXOs (PLL)

	SG-8018	SG-8101	SG-82xx
Frequency Range (MHz)	0.67 to 170	0.67 to 170	1.2 to 170
Frequency Options	1 Frequency (Fractional-N PLL)	1 Frequency (Fractional-N PLL)	1 Frequency (Fractional-N PLL)
Phase Jitter	<50ps RMS	<50ps RMS	1.1ps typ.
Supply Voltage	1.6V to 3.6V	1.6V to 3.6V	1.6V to 3.6V
Temperature Range	-40C to 105C	-40C to 85C -40C to 105C	-40C to 105C -40C to 125C
Frequency Tolerance	50 ppm TTL inc. 10years aging	15/20/50 ppm	15/20/50 ppm TTL inc. 1year aging
Current Consumption	2.7mA to 6.8mA	2.7mA to 6.8mA	7.5mA – 12.4mA
Output Type	LVC MOS	LVC MOS	LVCMS
Packages	CG/CE/CB/CA	CG/CE/CB/CA	CG/CJ

Any non-standard frequency with 6 digits behind the comma

Phase Jitter in the range of direct oscillators

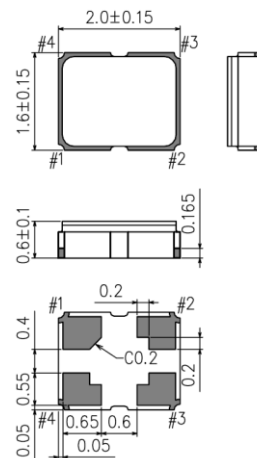
High Stability over wide temperature range

Most common footprints
Smallest = cheapest !

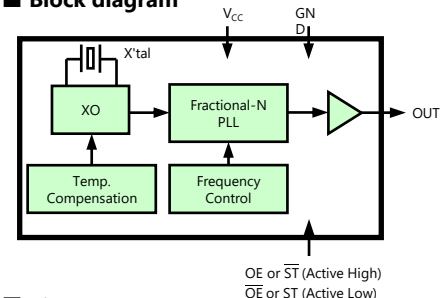
SG-8200CJ/SG-8201CJ - New Low Jitter PLL SPXO

Item	Specifications
Frequency (fo)	1.2 MHz to 170 MHz
Output	CMOS
Supply voltage (V _{CC})	1.62 V to 3.63 V
Frequency tolerance / Operating temperature	SG-8200CJ: $\pm 50 \times 10^{-6}$ / -40 °C to +125 °C SG-8201CJ: $\pm 15 \times 10^{-6}$ / -40 °C to +105 °C $\pm 25 \times 10^{-6}$ / -40 °C to +125 °C Including Initial frequency tolerance Frequency / temperature characteristics, Frequency / voltage coefficient, Frequency / load Coefficient and Aging (+25 °C, First year)
Current consumption	7.5 mA Max. (fo = 25 MHz) 12.4 mA Max. (fo = 125 MHz)
Symmetry	45 % to 55 %
Rise/Fall time	2.0 ns Max. (fo > 125 MHz) 2.5 ns Max. (75 MHz < fo ≤ 125 MHz) 4.0 ns Max. (50 MHz < fo ≤ 75 MHz) 6.0 ns Max. (fo ≤ 50 MHz)
Phase jitter (12 kHz to 20 MHz)	1.1 ps Typ. (fo = 125 MHz)
Function	Output enable or Stand-by

External dimension



Block diagram



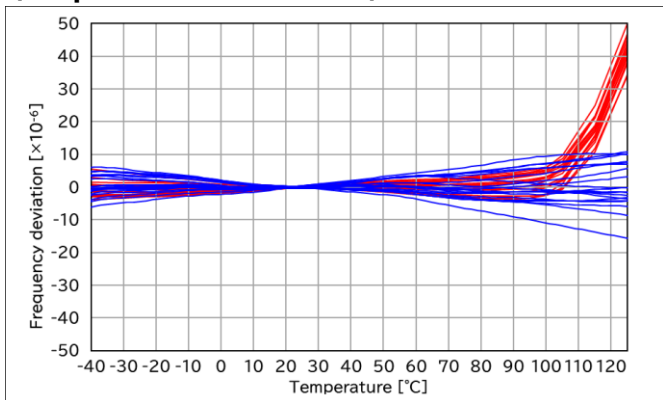
Pin map

#1	OE or ST (Active High) ST or OE (Active Low)
#2	GND
#3	OUT
#4	Vcc

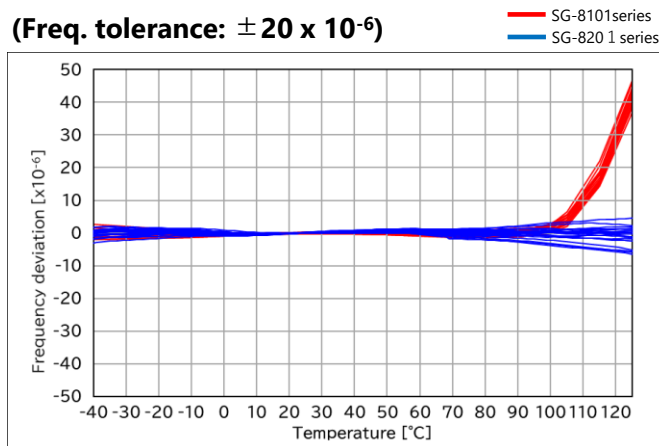
High Stability & Wide Temperature Range

Compared with existing programmable SPXO SG-8101series, this product can adjust the temperature variation up to +125 ° C and has high stability characteristics over a wide temperature range.

SG-8200CJ vs SG-8101series
(Freq. tolerance: $\pm 50 \times 10^{-6}$)



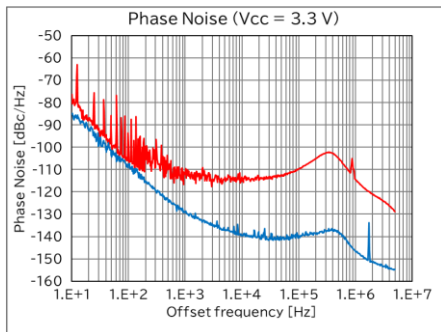
SG-8201CJ vs SG-8101series
(Freq. tolerance: $\pm 20 \times 10^{-6}$)



Low Phase Noise/Low Jitter Characteristics

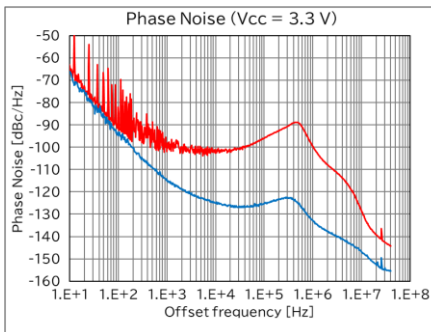
Compared with existing programmable SPXO SG-8101series, phase noise is improved about 30 dBc/Hz at offset frequency from 100 kHz to 1 MHz, and phase jitter is reduced to about 1/40.

fo = 25.0 MHz



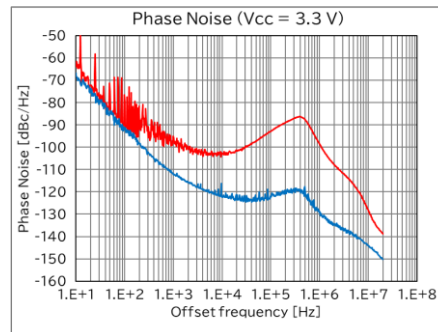
	Phase jitter (12 kHz to 5 MHz)
SG-8101series	45.8 ps
SG-8201series	1.2 ps

fo = 125.0 MHz



	Phase jitter (12 kHz to 20 MHz)
SG-8101series	43.7 ps
SG-8201series	1.1 ps

fo = 170.0 MHz



	Phase jitter (12 kHz to 20 MHz)
SG-8101series	42.3 ps
SG-8201series	1.5 ps

SPXO – CMOS with 5V operating voltage

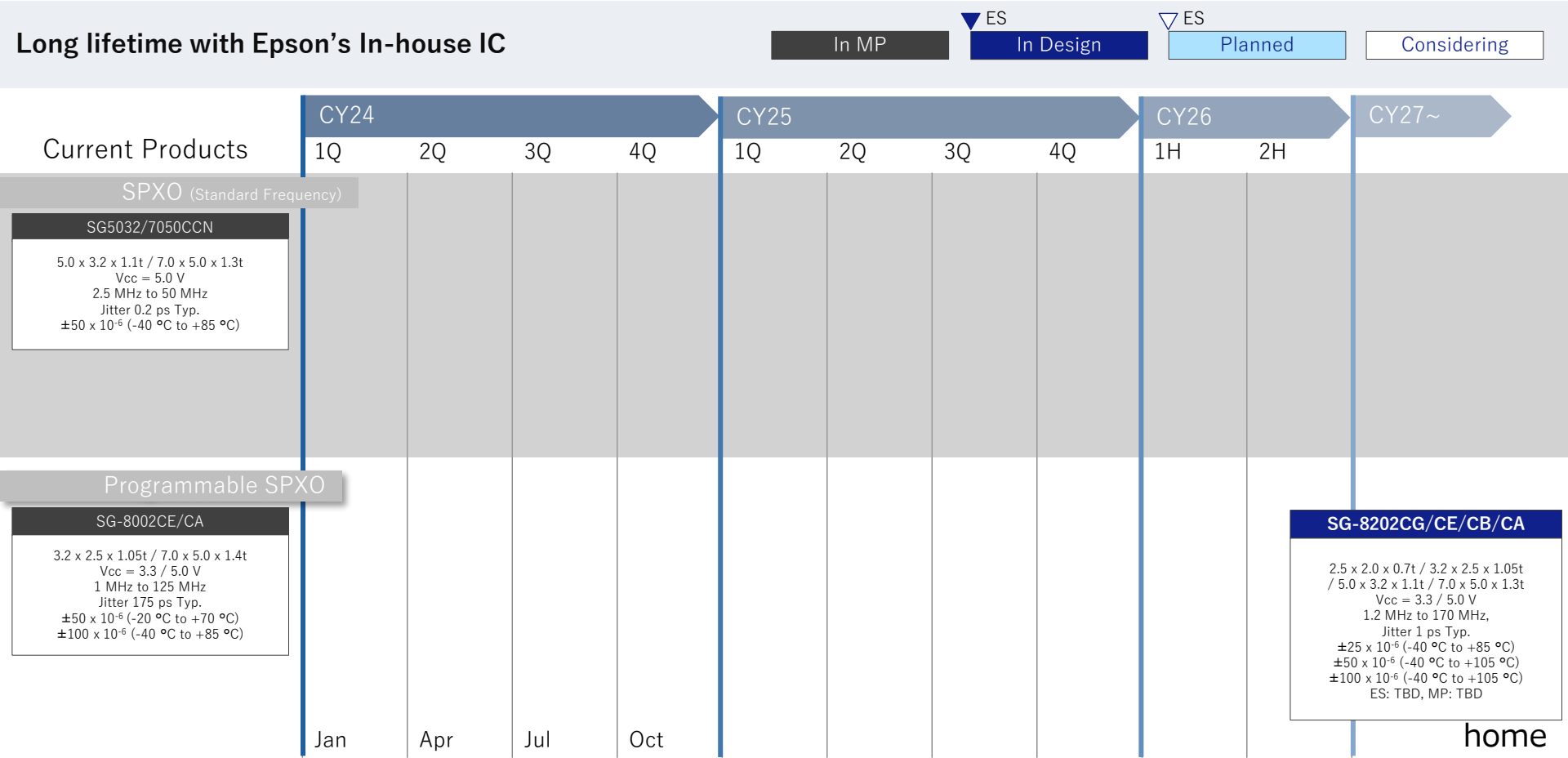
Long lifetime with Epson’s In-house IC

In MP

In Design

Planned

Considering



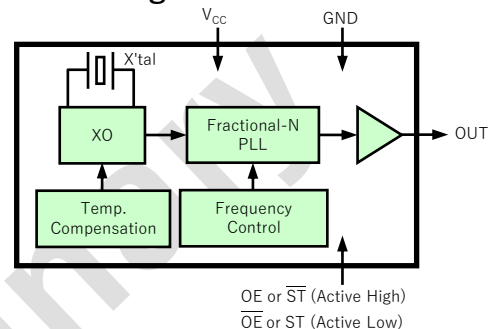
Feature

- **Low noise Fractional PLL technology** support **any frequency** between 1.2 MHz and 170 MHz with quick turn-around time
- $\pm 15 \times 10^{-6}$ (up to +105 °C) / $\pm 25 \times 10^{-6}$ (up to +125 °C) with **Temperature compensation function**

Specifications

Item	Specifications
Frequency (f ₀)	1.2 MHz to 170 MHz
Output	CMOS
Supply voltage (V _{CC})	2.25 V to 5.5 V
Frequency tolerance / Operating temperature	$\pm 15 \times 10^{-6}$ / -40 °C to +105 °C $\pm 25 \times 10^{-6}$ / -40 °C to +125 °C * Including includes Initial frequency tolerance, Frequency / temperature characteristics, Frequency / voltage coefficient, Frequency / load coefficient, and Aging (+25 °C, First year)
Current consumption (No load)	12 mA Max. (f ₀ = 25 MHz) 20 mA Max. (f ₀ = 125 MHz)
Symmetry	45 % to 55 %
Phase jitter (@125 MHz)	1 ps Typ. / 12 kHz to 20 MHz
Function	Output enable or Stand-by

Block diagram



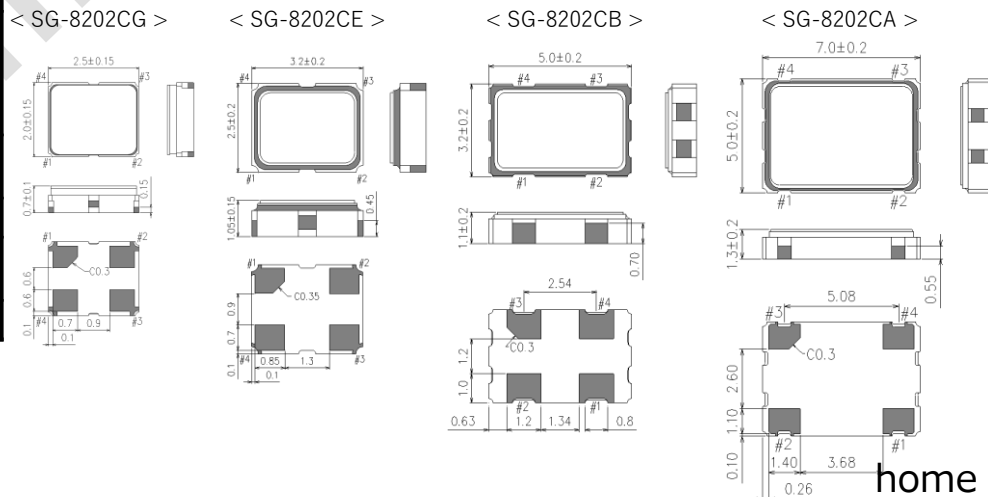
Schedule

ES: TBD
MP: TBD

Pin map

#1	OE or $\overline{ST}$ (Active High) ST or $\overline{OE}$ (Active Low)
#2	GND
#3	OUT
#4	Vcc

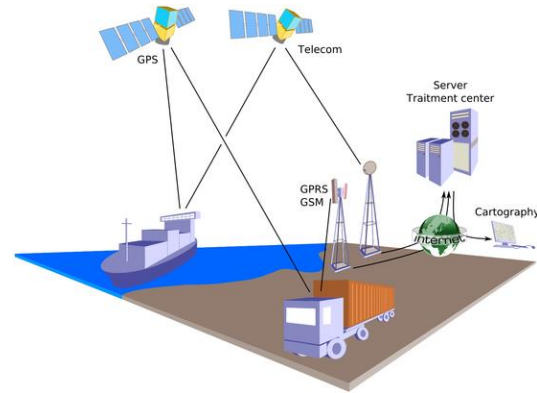
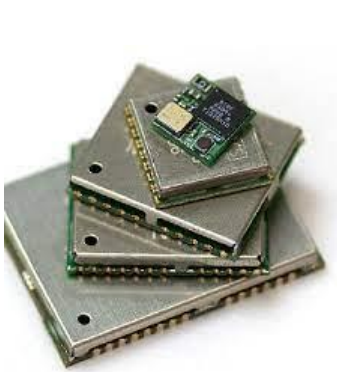
External dimension (unit in mm)



TCXO

Temperature Compensated Oscillators with Epson IC inside





- Temperature
- Compensated
- **X** = Crystal
- Oscillator

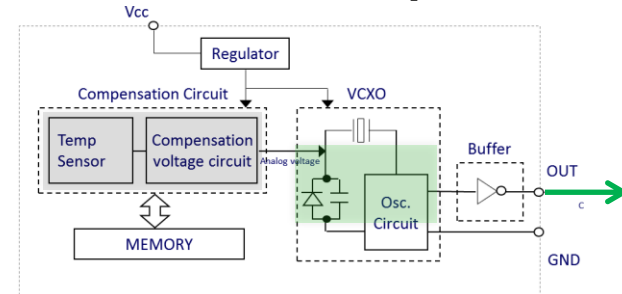
Important Specs

- Size
- Frequency
- Voltage
- +/-2ppm or +/-0.5ppm Stability
- Operating Temperature
- Voltage Control

Key Applications

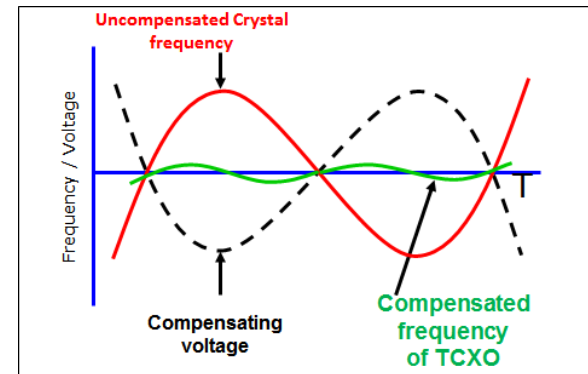
- GPS reference
- RF reference

Basic Principle



measure temperature, adjust frequency

TCXO output: Green curve



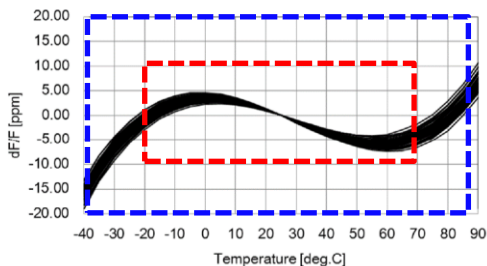
Reference: John Vig's Tutorial

home

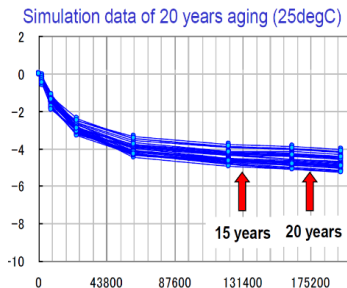
1

Tolerance at 25C

2



3



Component	-Stability / ppm	+Stability / ppm	
1 : 25C	-10	10	
2 : Temp	-20	20	-40+85C
3 : Ageing	-10	0	20 years
TOTAL	-40	+30	

But ... 20ppm 'total' stability is needed !

Solution : Go for Compensation
Choose a TCXO

Crystals vs TCXOs

MHz Crystal (50ppm)



TCXO (0.5ppm)



In MP

ES

In Design

ES

Planned

Considering

Current Products

For Industrial/Consumer

TG2016SMN/TG2520SMN

2.0 x 1.6 x 0.8t Max. / 2.5 x 2.0 x 0.9t Max.
10 MHz to 55 MHz
 $\pm 0.5 \times 10^{-6}$ (-40 °C to +85 °C)

TG2520CEN/TG3225CEN

2.5 x 2.0 x 0.9t Max. / 3.2 x 2.5 x 1.0t Max.
12 MHz to 52 MHz, CMOS output
 $\pm 2 \times 10^{-6}$ (-40 °C to +85 °C)

TG2016SLN

2.0 x 1.6 x 0.7t Max., ST function
10 MHz to 55.2 MHz
 $\pm 0.5 \times 10^{-6}$ (-40 °C to +85 °C)
 $\pm 5.0 \times 10^{-6}$ (+85 °C to +105 °C)

TG1612SLN

1.6 x 1.2 x 0.45t Max., ST function
26 MHz
 $\pm 0.5 \times 10^{-6}$ (-40 °C to +85 °C)
 $\pm 5.0 \times 10^{-6}$ (+85 °C to +105 °C)

For Automotive

TG2016SKA/TG2016SLA

2.0 x 1.6 x 0.7t Max.
13 MHz to 55 MHz,
AEC-Q100
SKA: $\pm 0.5 \times 10^{-6}$ (-40 °C to +105 °C)
SLA: $\pm 0.5 \times 10^{-6}$ (-40 °C to +85 °C)

CY25

1Q

2Q

3Q

4Q

Jan

Apr

Jul

Oct

CY26

1Q

2Q

3Q

4Q

TG2520SRN/CRN

2.0 x 1.6 x 0.7t Max., ST function
10 MHz to 80 MHz
 $\pm 0.5 \times 10^{-6}$ (-40 °C to +105 °C)
ES: 1st CY26, MP: 2nd CY26

TG2016SRN/CRN

2.5 x 2.0 x 0.8t Max., ST function
10 MHz to 80 MHz
 $\pm 0.5 \times 10^{-6}$ (-40 °C to +105 °C)
ES: 1st CY26, MP: 2nd CY26

TG1612SRN/CRN

1.6 x 1.2 x 0.55t Max., ST function
26/32/38.4/52/64/76.8 MHz
 $\pm 0.5 \times 10^{-6}$ (-40 °C to +105 °C)
ES: 1st CY26, MP: 2nd CY26

CY27

1H

2H

TG2016STN

2.0 x 1.6 x 0.7t Max., ST function
26/32/38.4 MHz
1.2V,
 $\pm 0.5 \times 10^{-6}$ (-40 °C to +105 °C)
ES: TBD, MP: TBD

TG1612STN

1.6 x 1.2 x 0.55t Max., ST function
26/32/38.4 MHz
1.2V,
 $\pm 0.5 \times 10^{-6}$ (-40 °C to +105 °C)
ES: TBD, MP: TBD

CY28~

TG1210SRN/CRN

1.2 x 1.0 x 0.5t Max., ST function
26/32/38.4/52/64/76.8 MHz
 $\pm 0.5 \times 10^{-6}$ (-40 °C to +105 °C)
ES: TBD, MP: TBD

TG1210STN

1.2 x 1.0 x 0.5t Max., ST function
26/32/38.4 MHz
1.2V,
 $\pm 0.5 \times 10^{-6}$ (-40 °C to +105 °C)
ES: TBD, MP: TBD

home

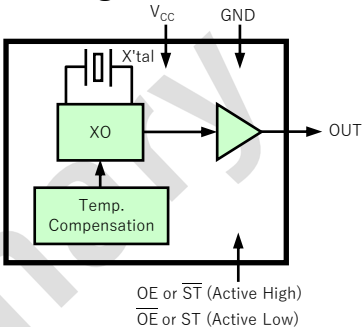
Feature

- High frequency stability in up to +105 ° C
- Tight symmetry
- Precise and Low phase noise

Specifications

Item	Specifications
Frequency (fo)	26, 32, 38.4, 39, 49.58, 52, 64, 76.8 MHz
Output	Clipped Sine / CMOS
Supply voltage (Vcc)	1.8 V ± 5 % / 2.5 V ± 10 % / 3.3 V ± 10 %
Frequency Tolerance	± 2.0 x 10 ⁻⁶ Max. / After 2 reflows, +25° C
Frequency temperature characteristics	± 0.5 x 10 ⁻⁶ Max. (opt. ± 0.28 x 10 ⁻⁶ Max.) / -40 ° C to +105 ° C
Current consumption (@26MHz)	1.5 mA Max. / -40 ° C to +105 ° C, 10kΩ/10pF
Symmetry	45 % to 55 % (opt. 49 % to 51 %)
Phase noise (@26MHz)	-92 dBc/Hz Typ. at 10 Hz -117 dBc/Hz Typ. at 100 Hz -138 dBc/Hz Typ. at 1 kHz -146 dBc/Hz Typ. at 10 kHz -152 dBc/Hz Typ. at 100 kHz -161 dBc/Hz Typ. at 1 MHz
Function	Output enable or Stand-by

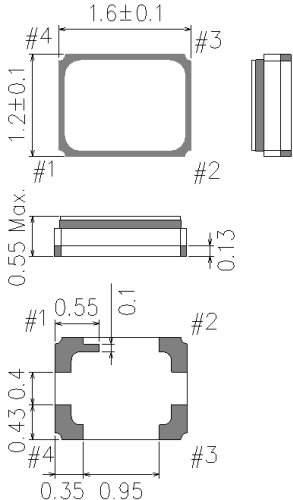
Block diagram



Schedule

ES: CY25/1Q
MP: CY25/2Q

External dimension (unit in mm)



Pin map

#1	OE or ST (Active High) ST or OE (Active Low)
#2	GND
#3	OUT
#4	Vcc

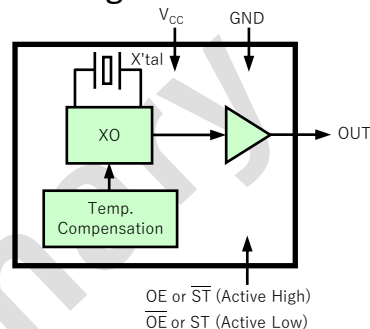
Feature

- High frequency stability in up to +105 ° C
- Tight symmetry
- Precise and Low phase noise

Specifications

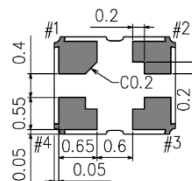
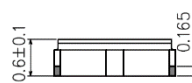
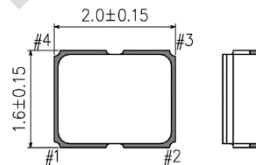
Item	Specifications
Frequency (fo)	26, 32, 38.4, 39, 49.58, 52, 64, 76.8 MHz
Output	Clipped Sine / CMOS
Supply voltage (V _{CC})	1.8 V ± 5 % / 2.5 V ± 10 % / 3.3 V ± 10 %
Frequency Tolerance	± 2.0 x 10 ⁻⁶ Max. / After 2 reflows, +25 ° C
Frequency temperature characteristics	± 0.5 x 10 ⁻⁶ Max. (opt. ± 0.28 x 10 ⁻⁶ Max.) / -40 ° C to +105 ° C
Current consumption (@26MHz)	1.5 mA Max. / -40 ° C to +105 ° C, 10kΩ/10pF
Symmetry	45 % to 55 % (opt. 49 % to 51 %)
Phase noise (@26MHz)	-92 dBc/Hz Typ. at 10 Hz -117 dBc/Hz Typ. at 100 Hz -138 dBc/Hz Typ. at 1 kHz -146 dBc/Hz Typ. at 10 kHz -152 dBc/Hz Typ. at 100 kHz -161 dBc/Hz Typ. at 1 MHz
Function	Output enable or Stand-by

Block diagram

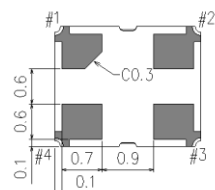
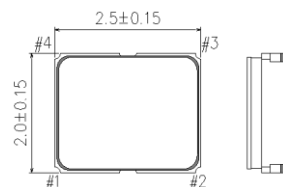


External dimension (unit in mm)

< TG2016SRN/CRN >



< TG2520SRN/CRN >



Schedule

TG2016SRN: ES: TBD
MP: TBD
TG2520SRN: ES: TBD
MP: TBD

Pin map

#1	OE or ST (Active High) ST or OE (Active Low)
#2	GND
#3	OUT
#4	Vcc

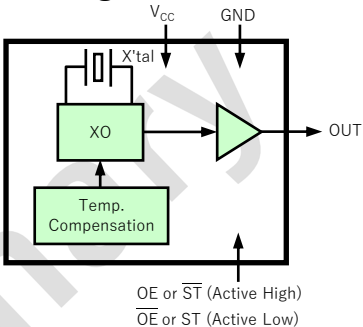
Feature

- High frequency stability in up to +105 ° C
- Tight symmetry
- Precise and Low phase noise

Specifications

Item	Specifications
Frequency (fo)	26, 32, 38.4, 39, 49.58, 52, 64, 76.8 MHz
Output	Clipped Sine / CMOS
Supply voltage (Vcc)	1.8 V ± 5 % / 2.5 V ± 10 % / 3.3 V ± 10 %
Frequency Tolerance	± 2.0 x 10 ⁻⁶ Max. / After 2 reflows, +25° C
Frequency temperature characteristics	± 0.5 x 10 ⁻⁶ Max. (opt. ± 0.28 x 10 ⁻⁶ Max.) / -40 ° C to +105 ° C
Current consumption (@26MHz)	1.5 mA Max. / -40 ° C to +105 ° C, 10kΩ/10pF
Symmetry	45 % to 55 % (opt. 49 % to 51 %)
Phase noise (@26MHz)	-92 dBc/Hz Typ. at 10 Hz -117 dBc/Hz Typ. at 100 Hz -138 dBc/Hz Typ. at 1 kHz -146 dBc/Hz Typ. at 10 kHz -152 dBc/Hz Typ. at 100 kHz -161 dBc/Hz Typ. at 1 MHz
Function	Output enable or Stand-by

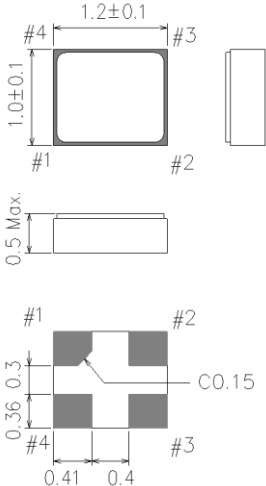
Block diagram



Schedule

ES: TBD
MP: TBD

External dimension (unit in mm)



Pin map

#1	OE or ST (Active High) ST or OE (Active Low)
#2	GND
#3	OUT
#4	Vcc

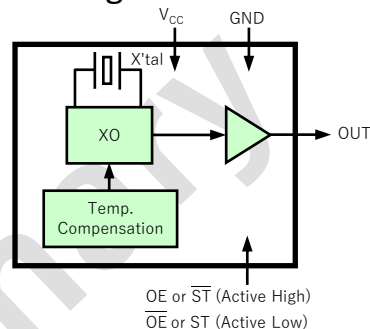
Feature

- Low supply voltage 1.1 to 1.3 V
- High frequency stability in up to +105 ° C
- Tight symmetry
- Precise and Low phase noise

Specifications

Item	Specifications
Frequency (fo)	10 MHz to 80 MHz
Output	Clipped Sine
Supply voltage (V _{CC})	1.1 ~ 1.3 V
Temperature slope	$\pm 0.1 \times 10^{-6} / ^\circ \text{C}$
Frequency temperature characteristics	$\pm 0.5 \times 10^{-6} \text{ Max.} / -40^\circ \text{C to } +85^\circ \text{C}$
Current consumption (@26MHz)	1.55 mA Max. / -40 ° C to +85 ° C, 10kΩ/10pF
Phase noise (@26MHz)	-83 dBc/Hz Max. at 10 Hz -108 dBc/Hz Max. at 100 Hz -130 dBc/Hz Max. at 1 kHz -145 dBc/Hz Max. at 10 kHz -148 dBc/Hz Max. at 100 kHz -148 dBc/Hz Max. at 1 MHz
Function	Output enable or Stand-by

Block diagram

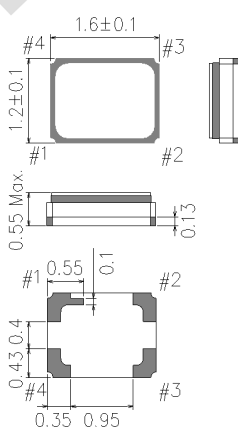


Schedule

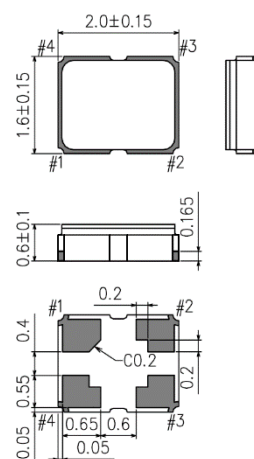
TG1612STN: ES: TBD
MP: TBD
TG2016STN: ES: TBD
MP: TBD

External dimension (unit in mm)

< TG1612STN >



< TG2016STN >



Pin map

#1	OE or ST (Active High) ST or OE (Active Low)
#2	GND
#3	OUT
#4	Vcc

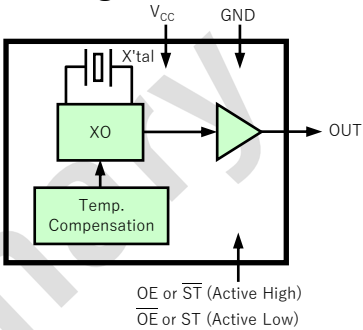
Feature

- Low supply voltage 1.1 to 1.3 V
- High frequency stability in up to +105 ° C
- Tight symmetry
- Precise and Low phase noise

Specifications

Item	Specifications
Frequency (fo)	10 MHz to 80 MHz
Output	Clipped Sine
Supply voltage (Vcc)	1.1 ~ 1.3 V
Temperature slope	±0.1 x 10 ⁻⁶ /° C
Frequency temperature characteristics	±0.5 x 10 ⁻⁶ Max. / -40° C to +85° C
Current consumption (@26MHz)	1.55 mA Max. / -40° C to +85° C, 10kΩ/10pF
Phase noise (@26MHz)	-83 dBc/Hz Max. at 10 Hz -108 dBc/Hz Max. at 100 Hz -130 dBc/Hz Max. at 1 kHz -145 dBc/Hz Max. at 10 kHz -148 dBc/Hz Max. at 100 kHz -148 dBc/Hz Max. at 1 MHz
Function	Output enable or Stand-by

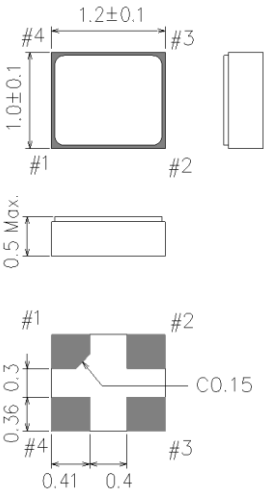
Block diagram



Schedule

ES: TBD
MP: TBD

External dimension (unit in mm)



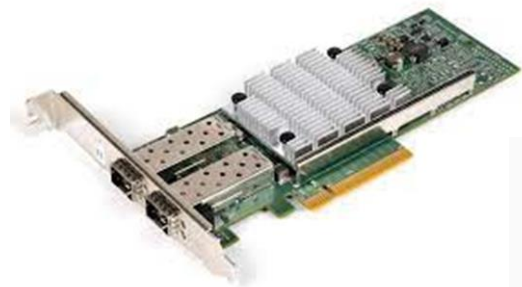
Pin map

#1	OE or ST (Active High) ST or OE (Active Low)
#2	GND
#3	OUT
#4	Vcc

Networking Special

High end SPXO / TCXO / VCXO / OCXO





400G QSFP-DD SR8



400G QSFP-DD AOC



SPXO / SPSO

kHz SPXO

MHz SPXO

P-SPXO

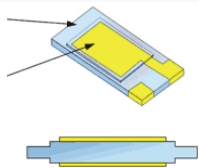
SPSO

Tuning Fork
Crystal



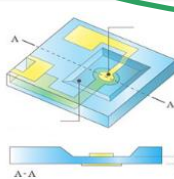
- Freq: 32.768kHz
- Output: CMOS

AT-Cut
Crystal



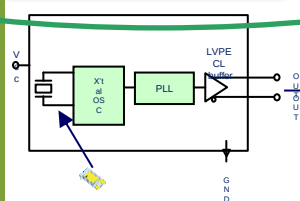
- Freq: 1 to 75MHz
- Output: CMOS

HFF
Crystal



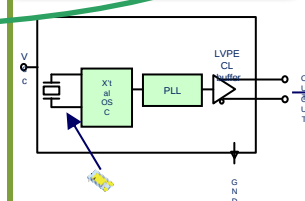
- HFF = (High Frequency Fundamental)
- Freq: up to 500MHz
 - Output:
(LVDS, LVPECL, HCSL, CMOS)

AT + PLL



- Freq: 50 to 800MHz
- Output: Differential
(LVDS, LVPECL, HCSL)

AT + PLL



- Freq: 0.67 to 170MHz (Surface Acoustic Wave)
- & 50 to 800MHz
- Outputs: (CMOS, LVPECL)
- Freq: 50 to 700MHz
- Differential Output
(LVDS, LVPECL, HCSL, CMOS)

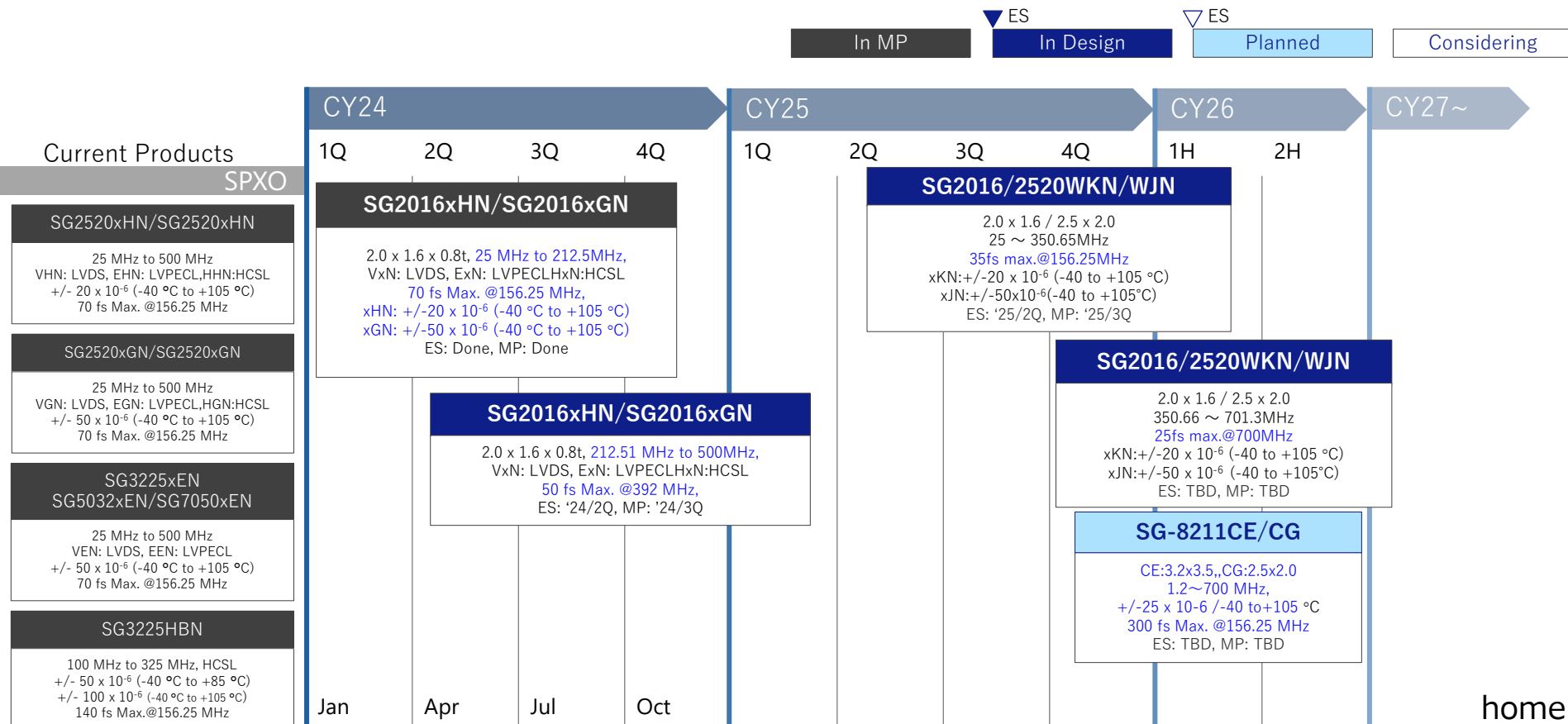
SAW



PHASE IN

PHASE OUT

home



Features

- High Frequency up to 500MHz
- Low jitter 60fs max. @156.25MHz (LVDS, Vcc=3.3V/2.5V)
- High stability $\pm 20\text{ppm}$, 50ppm (Including 10 years aging)
- Built-in Fundamental Crystal
- Output : LVPECL, LVDS, HCSL
- Small SMT Package 2.0 x 1.6mm (t=0.75mm max.)

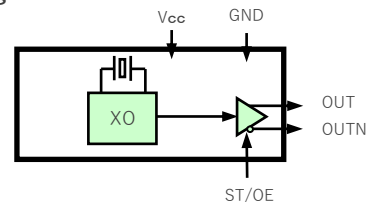
Applications

- 40G/100G/400G PHP, 400G-ZR, 800G-ZR
- Router/Switch, Server, Storage

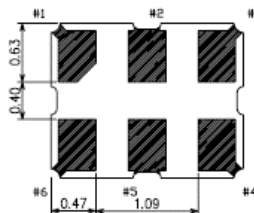
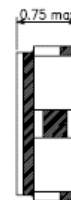
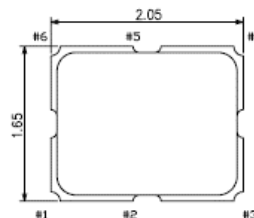
Specifications

Item	Specifications
Output Frequency	25 to 500MHz
Frequency stability (incl. calibration tolerance, temperature, supply voltage variations, and 10years aging at +25°C)	xHN : $\pm 20 \times 10^{-6}$ xGN : $\pm 50 \times 10^{-6}$
Operating temperature	-40C to +85C (Option: -40 to +105°C)
Current consumption	60mA max. (LVPECL) 28mA max. (LVDS) 40mA max.(HCSL)
Supply voltage	3.3V / 2.5V / 1.8V (LVDS only)
Output	LVPECL / LVDS / HCSL
Symmetry	45 % to 55 %
Phase jitter (12kHz to 20MHz, 3.3V)	44fs Typ. (156.25MHz; LVPECL) 38fs Typ. (156.25MHz; LVDS) 57fs typ. (100.00MHz ; HCSL)

Block Diagram



Package and Pin Assignments



Pin	Connections
#1	ST/OE
#2	NC
#3	GND
#4	OUT
#5	OUTN
#6	VCC

Schedule

ES : Done (~212.5M)
 '24/2Q (212.5M~500)
 MP: Done (~212.5M)
 '24/3Q (212.5M~500)

home

Features

- High Frequency up to 700MHz
- Low jitter 35fs max. @156.25MHz (Vcc=3.3V/2.5V)
- High stability $\pm 20\text{ppm}, 50\text{ppm}$ (Including 10years aging)
- Built-in Fundamental Crystal
- Output : WA-LVDS (Wide amplitude LVDS, VOD:0.35 to 0.8V)
- Small SMT Package 2.5x2.0, 2.0 x1.6mm
- The basic specifications are the same as the SG2502xGN/xHN

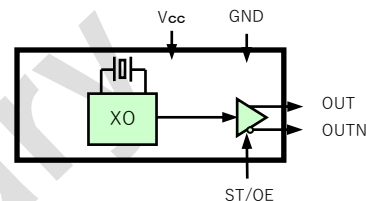
Applications

- 1.6T PHY , 1.6T-ZR
- Router/Switch, Server, Storage

Specifications

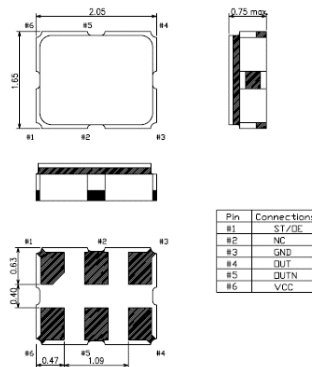
Item	Specifications
Output Frequency	25 to 700MHz
Frequency stability (incl. calibration tolerance, temperature, supply voltage variations, and 10years aging)	WKN : $\pm 20 \times 10^{-6}$ WJN : $\pm 50 \times 10^{-6}$
Operating temperature	-40C to +85C (Option: -40 to +105C)
Current consumption	60mA max. (762.5mV) 28mA max. (350mV) 40mA max.(800mV)
Supply voltage	3.3V / 2.5V / 1.8V (0.35mV)
Output	WA-LVDS
Output option(WA-LVDS) Offset voltage switching	350 to 800mV 0.9V/1.25V/1.5V/1.64V
Symmetry	45 % to 55 %
Phase jitter (12kHz to 20MHz, 3.3V)	35fs Max. (156.25MHz)

Block Diagram

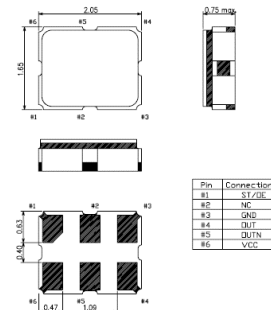


Package and Pin Assignments

[2.5x2.05]



[2.0x1.6]



Schedule

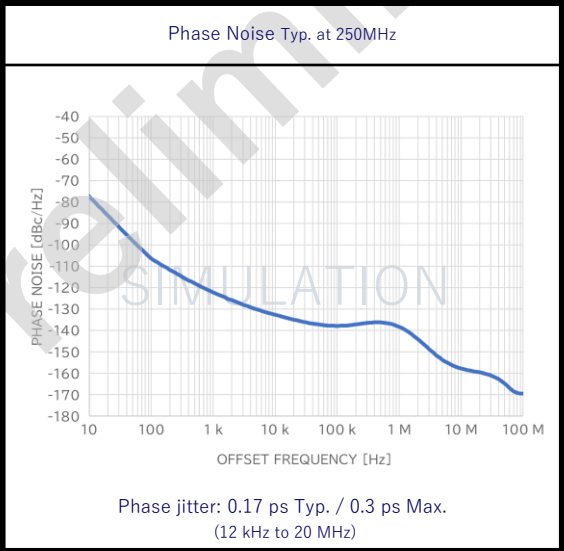
ES : '25/2Q (~350.65M)
TBD (350.67~700M)

Features

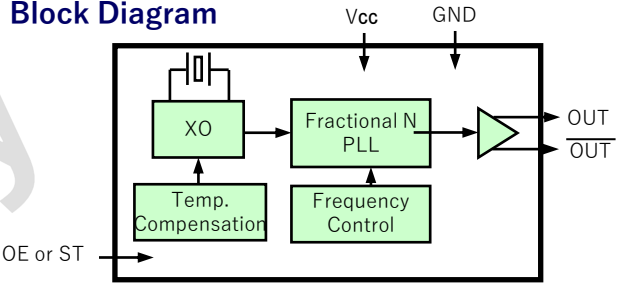
- Low jitter 0.3 ps Max.
- +/-50 ppm high stability @-40 ° C to +125 ° C
- Output option
 - LVDS with 10 amplitude options
 - includes LVPECL compatible differential amplitude with LVDS termination
 - HCSL
- CGA: 2.5 x 2.0 x 0.85t, CEA: 3.2 x 2.5 x 1.2t

Target Specifications

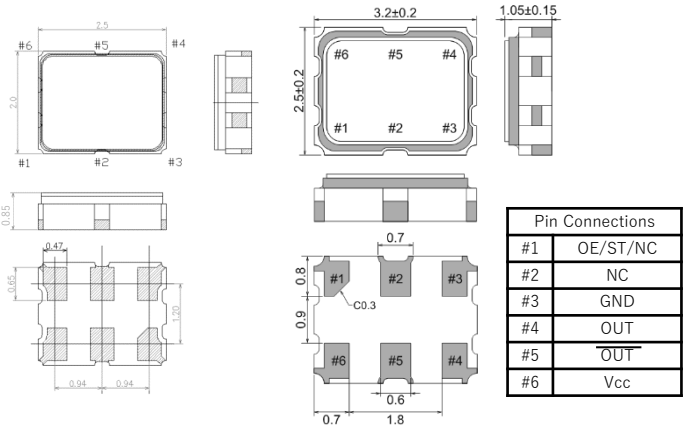
Item	Specifications
Output Frequency	3.52 MHz to 700 MHz (Option: to 1 GHz)
Frequency stability	+/-20 ppm at -40 ° C~+85 ° C +/-25 ppm at -40 ° C~+105 ° C +/-50 ppm at -40 ° C~+125 ° C incl. calibration tolerance, temperature, supply voltage variations, reflow drift, load drift and 10 years aging at +25 ° C.
Current consumption	36 mA Max. LVDS 42 mA Max. LVPECL compatible 38 mA Max. HCSL (Vcc=2.5V, @200MHz)
Supply voltage	1.71V~3.63V
Symmetry	45 % to 55 %



Block Diagram



Package and Pin Assignments



Schedule
ES : TBD
MP: TBD

home

Wide Operating Temperature range

▼ ES

▽ ES

In MP

In Design

Planned

Considering

Current Products

TCXO

TG-5510CA
TG-5511CA

7.0 x 5.0, 10 MHz to 54 MHz, 3.3 V
CMOS / Clipped sine wave
+/- 250 x 10⁻⁹ (-40 °C to +105 °C)
TG-5510CA: 10 pin, TG-5510CA: 4 pin

TG7050CKN/SKN
TG7050CMN/SMN

7.0 x 5.0, 10 MHz to 54 MHz, 3.3 V
CxN: CMOS, SxN: Clipped sine wave
+/- 100 x 10⁻⁶ (-40 °C to +105 °C)
Temp. slope: +/- 50 x 10⁻⁹ / °C
TG7050xKN: 10 pin/TG7050xMN: 4 pin

TG5032CGN/SGN
TG5032CFN/SFN

5.0 x 3.2, 10 MHz to 40 MHz, 3.3 V
CxN: CMOS, SxN: Clipped sine wave
+/- 100 x 10⁻⁶ (-40 °C to +85 °C)
TG5032xGN: 10 pin/TG5032xFN: 4 pin

CY24

1Q 2Q 3Q 4Q

TG-5510CB/TG-5511CB

5.0 x 3.2, 10 MHz to 54 MHz, 3.3 V
CMOS / Clipped sine wave
+/- 250 x 10⁻⁹ (-40 °C to +105 °C)
TG-5510CB: 10 pin, TG-5511CB: 4 pin
ES: Done, MP: Done

TG5032CKN/TG5032SKN
TG5032CMN/TG5032SMN

5.0 x 3.2, 10 MHz to 54 MHz, 3.3V
+/- 100 x 10⁻⁹ (-40 °C to +105 °C)
Temp. slope: +/- 50 x 10⁻⁹ / °C,
CKN: CMOS, 10 pin, SKN: Clipped sine wave, 10 pin
CMN: CMOS, 4 pin, SMN: Clipped sine wave, 4 pin
ES: Done, MP: Done

Jan

Apr

Jul

Oct

CY25

1Q 2Q 3Q 4Q

CY26

1H 2H

CY27~

TG7050/5032xxN/xxN

TCXO / VC-TCXO
7.0 x 5.0 / 5.0 x 3.2
10 to 96 MHz, 3.3 V
+/- 100 x 10⁻⁹ / -40 to +105 °C
Phase noise at floor
-170 dBc/Hz Max.
ES: TBD MP: TBD

OG7050xAN

7.0 x 5.0
1 to 170 MHz, 3.3 V
+/- 3 ~ 20 x 10⁻⁹ / -40 to 105 °C
≤ +/- 0.5 ppb/day
ES: TBD MP: TBD

home

TG7050/5032xxx – Low noise VC-TCXO

Features

- Frequency range 10MHz to 96MHz
- Low Phase Noise -167dBc/Hz @floor (challenge:-173dBc/Hz @floor)
- High stability ±100ppb / -40 to 85 °C (option 105 °C)
- Low Temperature Slope ±50ppb/ °C
- Output : CMOS / Clipped sine wave
- Small SMT Package 5.0 x 3.2mm (t=1.65mm max.)
7.0 x 5.0mm (t=1.70mm max.)

Applications

- BTS(RU), Server, PTP(IEEE1588), SyncE
- Router/Switch, Small cell

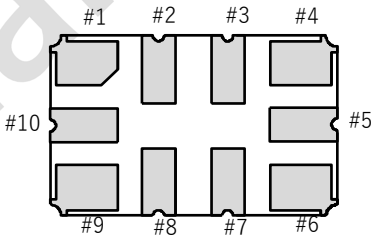
Target specifications

Item	Specifications
Output Frequency	10MHz to 96MHz
Frequency/Temperature Characteristics	±100ppb
Operating temperature	-40C to +85C (option 105°C)
Frequency Temperature Slope	±50ppb/°C
Aging	<±4.6ppm/10years
Current consumption	10mA max.
Supply voltage	3.3V
Output	CMOS / Clipped sine
Duty	49 to 51%
Start-up time	10 msec max. (Time required for output level to reach 90% Vcc or more)
Phase noise	-167dBc / floor challenge -173dBc / floor

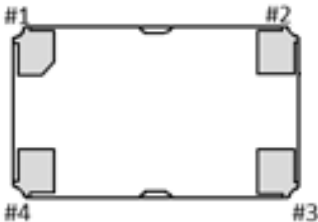
Bottom View

5.0 x 3.2mm

【10pin】



【4pin】



Pin Assignments

Pin	Connection
1	N.C. or Vc
2,5,8,10	N.C. Epson use only
3	OE
4	GND
6	OUT
7	N.C. or Filter
9	Vcc

Pin	Connection
1	N.C. or Vc
2	GND
3	OUT
4	Vcc

Schedule
ES : TBD
MP: TBD

Note) Values are result of simulations in development. The contents may change without notice.

Features

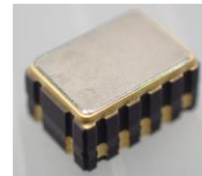
- High Frequency up to 170MHz [PLL technology](#)
- Low Phase Noise -155dBc/Hz @floor (Option:-160~-165dBc/Hz @floor) Jitter clean
- High stability $\pm 3 \sim 20$ ppb / -40 to 95 °C (option 105 °C)
- Output : CMOS
- Absolute Pull Range ± 5 ppm min. ([Digital control \(I2C\)](#))
- Small SMT Package 7.0 x 5.0mm (t=3.3mm max.)

Applications

- BTS(DU/RU), Server, PTP(IEEE1588)
- Router/Switch

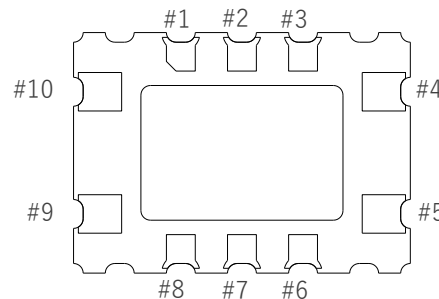
Target specifications

Item	Specifications
Output Frequency	1 to 170MHz
Frequency/Temperature Characteristics	$\pm 3 \sim 20$ ppb
Operating temperature	-40C to +95C (option 105°C)
Frequency Temperature Slope	$\pm 0.1 \sim 2.0$ppb/°C
Aging	$< \pm 0.5$ppb/day
Absolute Pull Range	± 5 ppm min. (Digital control/I2C)
Holdover	TBD (Target: 1.5us/6H)
Current consumption	400mA max. (during warm-up) 200mA max. (steady state)
Supply voltage	3.3V
Output	CMOS
Warm-up time	± 20 ppb / 30sec max. (After 1 hour on)
Phase noise	A (Standard) : -155dBc / floor B (Low noise) : -165dBc / floor



7.0 x 5.0mm (t=3.3mm max.)

Bottom View



Pin Assignments

Pin	Connection
1,2,3, 6,7,8	N.C. Epson use only
4	GND
5	OUT
9	Vcc
10	N.C. or Vc

Schedule
ES : TBD
MP: TBD

Note) Values are result of simulations in development. The contents may change without notice.

home

High Frequency, Small Size with Low C/N

▼ ES

In MP

In Design

▽ ES

Planned

Considering

Current Products

VCXO

VG3225xFN

3.2 x 2.5, 5.0 x 3.2
100 MHz to 392 MHz
-149 dBc/Hz Typ.
@10 kHz (122.88 MHz)
VFN: LVDS, EFN: LVPECL

VG5032xFN
VG7050xFN

5.0 x 3.2, 7.0 x 5.0
100 MHz to 250 MHz
-149 dBc/Hz Typ.
@10 kHz (122.88 MHz)
VFN: LVDS, EFN: LVPECL

CY24

1Q 2Q 3Q 4Q

VG3225xFN

3.2 x 2.5
392 MHz to 500 MHz
VFN: LVDS, EFN: LVPECL
-139 dBc/Hz Typ. @10 kHz (491.52 MHz)
ES: done, MP: TBD

Jan

Apr

Jul

Oct

CY25

1Q 2Q 3Q 4Q

CY26

1H 2H

CY27~

VG2520/3225xJN

~700MHz
Phase noise at floor
-167 dBc/Hz Max.
ES: TBD, MP: TBD

home

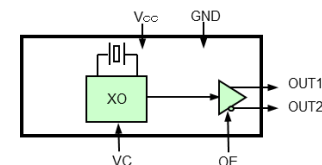
Features

- High Frequency up to 500MHz
- Low Noise
- Fundamental oscillation
- Small SMT Package 3.2 x 2.5 mm (t=0.75mm max.)
- +105°C high temperature (Option)
- LV-PECL(EFN) / LVDS(VFN) Output

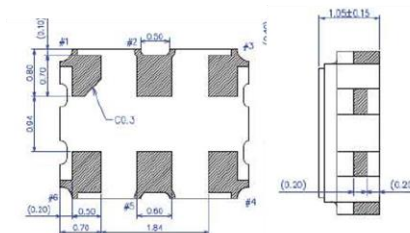
Specifications

Item	Specifications	Conditions / Remarks
Operating temp range	-40C to +85°C	-40 C to +105 °C (Option)
Output freq. range	25 to 500MHz	250~500MHz: under designing
Supply voltage	3.3 V $\pm$ 0.165 V	
Current consumption	LV-PECL: 60mA Max. LVDS : 30mA Max	EFN : LV-PECL VFN : LVDS
Freq. tolerance	± 50 ppm Max.	Includes initial tolerance, temperature change, Vcc change and 10years aging at +25°C.
Absolute Pull range	± 10 ppm Min	Vc= 0 V to 3.3 V reference to f0
Input resistance	10 M Ω Min.	DC level
Output load condition	50 Ω	LVPECL: Vcc-2.0V
Differential Output Voltage	Voh: Vcc-1.1V Min. Vol: Vcc-1.5V Max.	
Symmetry	45 % to 55 %	At outputs crossing point
Rise/Fall times	0.5 ns Max.	At 20 % to 80 % of output swing
High input voltage	70% Vcc	VIH or OPEN => Enable
Low input voltage	30% Vcc	VIL or GND => Disable
Oscillation start up time	10ms Max.	

Block Diagram



Package and Pin Assignments



Pin Connections	
#1	VC
#2	OE
#3	GND
#4	OUT
#5	OUTN
#6	Vcc

home

Phase noise(LV-PECL)

Offset frequency	122.88MHz	245.76MHz	491.52MHz
10Hz	-74dBc/Hz	-68dBc/Hz	-55dBc/Hz
100Hz	-104dBc/Hz	-100dBc/Hz	-86dBc/Hz
1kHz	-127dBc/Hz	-126dBc/Hz	-116dBc/Hz
10kHz	-149dBc/Hz	-146dBc/Hz	-141dBc/Hz
100kHz	-160dBc/Hz	-157dBc/Hz	-150dBc/Hz

Clock Buffers ICs



Clock Generator IC

- Generate multiple Clock signals with different frequencies based on the input Clock signal

Clock Buffer IC

- Distribute multiple Clock signals with the same frequencies as the input Clock signal

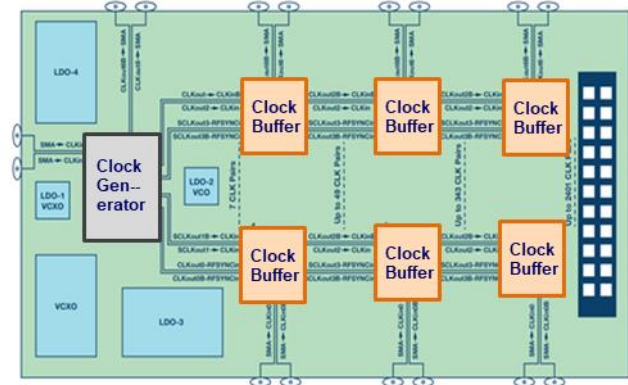
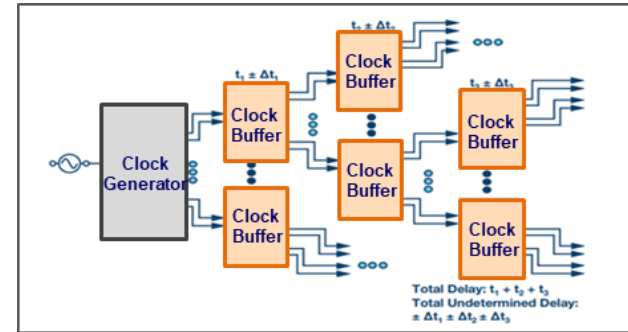
Necessity of Clock Buffer IC

- A single Clock Generator IC may not have enough outputs to drive all required Clock signals.
- Clock Buffers provide enough outputs and help synchronize multiple devices or systems.

Challenges and Solutions

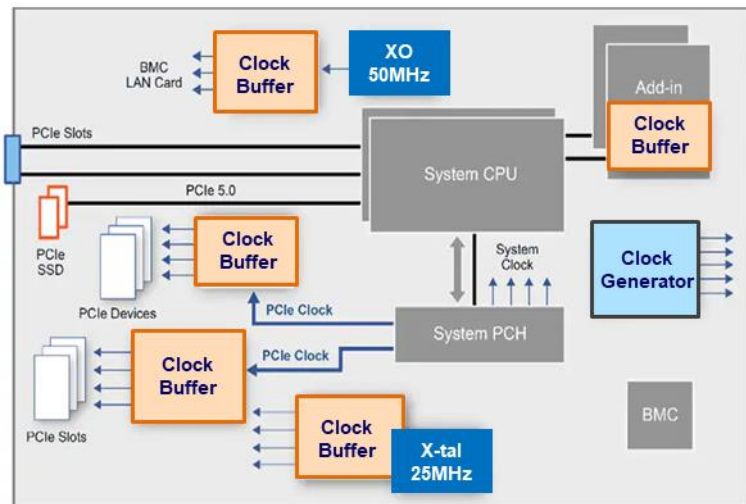
- Each stage in the clock tree causes a timing delay, influenced by temperature changes, voltage variations, etc
- Accumulated inaccuracies can lead to intolerable timing variations

Clock tree block diagram

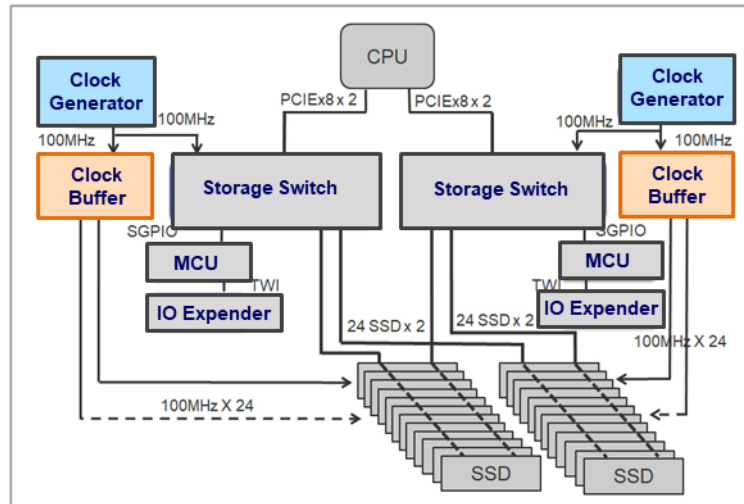


- PCIe Gen-1/2/3/4/5/6 Clock Distribution
- PCIe Graphics Cards
- PCIe Based SSD Switches and Drives
- Data Centers & Gigabit Ethernet
- Servers: Micro server, tower server, rack server and FBDIMM (Fully Buffered Dual Inline Memory Module)
- Communication switches
- Network Storages & Host Bus Adapter (HBA) cards

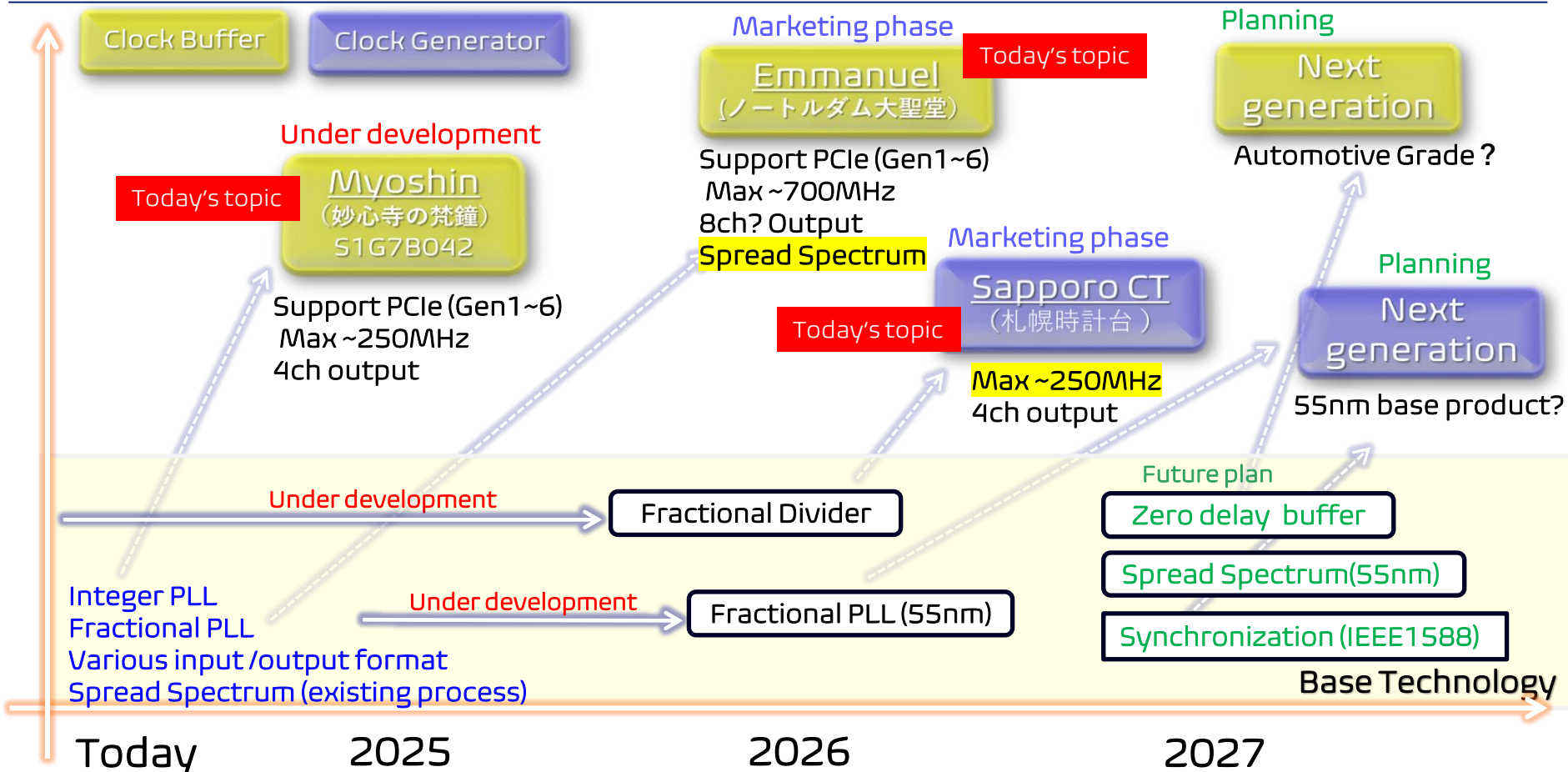
Typical Server Application with PCIe



NVMe SSD Switch Application



Roadmap (Clock solution)



Epson 4-Output Clock Buffer: Myoshin (S1G7B042)

EPSON

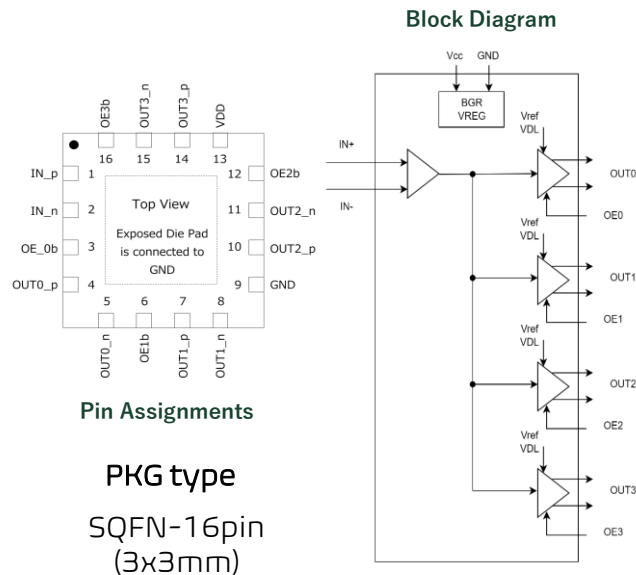
- 3 x 3 mm Tiny size
- Low jitter and Low skew
- Wide range of Operating temperature

PCIe	Gen 1~Gen6
Power supply	1.8V ± 5%, 2.5V ± 10%, 3.3V ± 10%
Operation Freq range	~ 250MHz
Input (format)	Option A: • DC-Coupled: HCSL, LP-HCSL • AC-Coupled: PECL, LVDS, CML, CMOS Option B • DC-Coupled: LVDS, WA-LVDS
Output (format)	LP-HCSL (Max 4 outputs)
Operating Temperature	-40C~105C (Operation)
Power consumption	Core device current : T.B.D (Target 13 mA) Output current (100 Ω termination) : T.B.D (Target 3.9mA) ※Per 1 output Output current (85 Ω termination) : T.B.D (Target 4.4mA) ※Per 1 output
Slew rate	0.6 V/ns ~ 4.0 V/ns
Additive Jitter	TBD (target 30fs? 12Khz~20MHz)
Output Skew	30ps
Duty	45%~55% (Input Duty 50%)

Under development

TS : Q4/25

MP : Q1/26

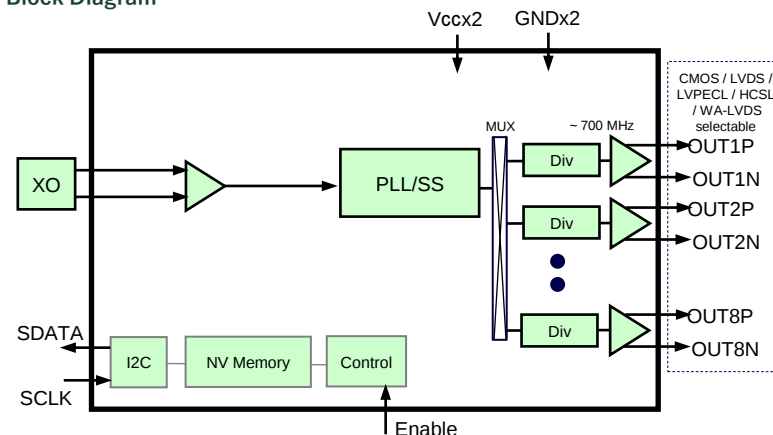


P2P compatible to Microchip SY75604

Multi output Clock buffer with Higher freq range (~700MHz)

Part # : S1Gxxx	
Power supply	1.8V $\pm$ 5%, 2.5V $\pm$ 10%, 3.3V $\pm$ 10%
Operation Freq range	~ 700MHz?
Output Ports	Max 4~16?
Output (format)	TBD LVPECL, LVDS? Or WA-LVDS? (*1)
Temperature range	-40C~105C (Operation) -65C~150C (Storage)
Power consumption	TBD
Slew rate	TBD
Additive Jitter	TBD (target 30fs? 12Khz~20MHz)
Output Skew	30ps (In part skew 50ps)
Spread spectrum	Yes?
PKG type	TBD

Block Diagram



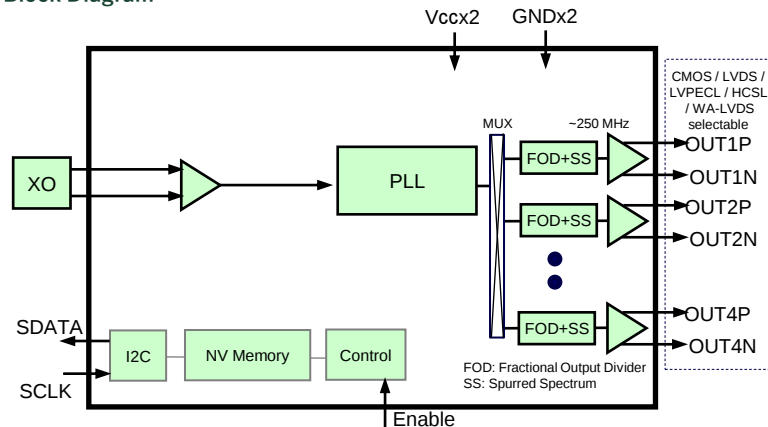
(*1) Wide amplitude LVDS

home

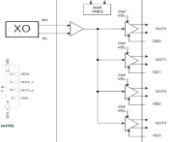
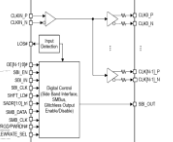
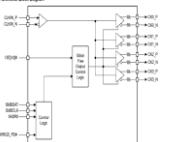
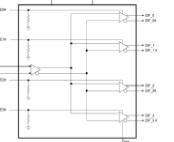
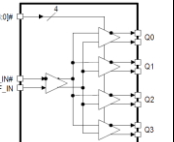
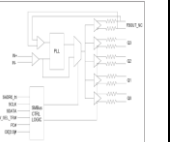
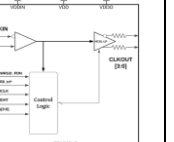
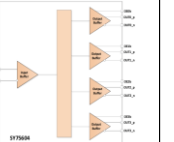
1st Clock Generator product 4 output with Higher freq range up to (~250MHz)

Part #: S1Gxxx	
Power Supply	1.8V $\pm$ 5%, 2.5V $\pm$ 10%, 3.3V $\pm$ 10%
Operation Freq range	~ 250MHz?
Output Ports	max 4
Output (format)	TBD? Selectable? (HCSL, LP-HCSL, CMOS, LVDS, WA-LVDS(Wide amplitude LVDS))
Temperature range	-40C~105C (Operation) -65C~150C (Storage)
Spread Spectrum	Yes
Additive Jitter	TBD
Other	*Programmable (FAMOS base) *Fractional Divider
Power consumption	TBD
PKG type	TBD

Block Diagram



Comparison: 4CH - HCSL / LP-HCSL Output

Key Features	Epson	TI	TI	ONSEMI	Renesas	Diode	SiTime	Microchip
Part name	S1G7B042 (Myoshin)	LMKDB1104 (NEW)	CDCDB400	NB3L204K	9INT31H400	PI6CBE33045	SiT92314	SY75604
PCIe Compliant	Gen 1~Gen6	Gen 1~Gen6	Gen 1~Gen6	Gen 3, Gen 4	TBC	Gen 1~Gen6	Gen 1~Gen6	Gen 1~Gen6
Power supply Typ.	1.8V, 2.5V, 3.3V	1.8V, 3.3V	3.3V Typ	2.5 V, 3.3 V	4.6V Max	3.3V Typ	3.3V Typ	1.8V, 2.5V, 3.3V Typ
Freq range	250MHz Max.	400MHz Max.	250MHz Max.	350MHz Max.	350MHz Max	400MHz Max	400MHz Max	250MHz Max
Input CH	1	1	1	1	1	1	1	1
Output CH	4	4	4	4	4	4	4	4
Output (Format)	LP-HCSL	LP-HCSL	LP-HCSL	HCSL	LP-HCSL	LP-HCSL	LP-HCSL	LP-HCSL
Logic control	No (EN pin)	Yes	Yes	No (EN pin)	No (EN pin)	Yes	Yes	No (EN pin)
Operating Temp.	-40C~105C	-40C~105C	-40C~105C	-40C~85C	-40C~85C	-40C~85C	-40C~85C	-40C~105C
SBI (Side Band Interface)	No	Yes	No	No	No	No	No	No
LOS (Loss of Signal) input detection	No	Yes	No	No	No	No	No	No
Additive Jitter (12Khz~20MHz)	TBD (target 30fs?)	31fs RMS Max. @ 156.25MHz	38fs RMS Max.	80fs RMS Max.	61fs RMS Typ. @ 156.25MHz	110fs RMS Max.	10 fs RMS Typ. After DB800Z filter	68fs RMS Max. @ 100MHz
Skew (Output-to-output)	30ps	50ps Max	50ps Max	100ps Max	40ps Typ.	50ps Max	50ps Pyp	50ps Max
Duty	45%~55%	45%~55%	40%~60%	45%~55%	45%~55%	45%~55%	TBC	48%~52%
PKG type	16pin-SQFN (3x3mm)	28pin-VQFN (4x4mm)	32pin-VQFN (5x5mm)	24pin-VQFN (4x4mm)	24pin-VFQFN (4x4mm)	32pin-TQFN (5x5mm)	32pin-VQFN (5x5mm)	16pin-VQFN (3x3mm)
Compliance	??	DB2000QL	DB800ZL	DB400H	DB400H			
Block Diagram								

Product	1 st sample	MP Qualification
Myoshin (4 output CB)	Oct CY2025	Dec CY2025
Emmanuel (8-16 output CB)	Early CY2026	Within CY2026
Sapporo CT (4 output CG)	Early CY2026	Within CY2026

Automotive Grade for Industry

AECQ-200/100 quality for

- > 125°C operation
- > Long lifetime
- > harsh environments



❖ Features:

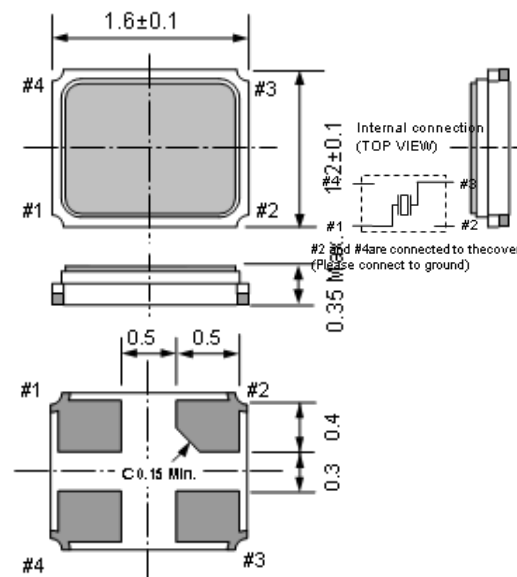
- Very small package size, best for small size requirements
- Temperature range from -40 to +125°C
- 1612 Package
- AEC-Q200

❖ Applications:

- Car accessories, Camera, Telematics, and Smart key,

Item	Specifications
Nominal frequency range	24 MHz to 80 MHz
Storage temperature range	-40 °C to +125 °C
Operating temperature range	-40 °C to +125 °C
Frequency tolerance(standard)	$\pm 10 \times 10^{-6}$
Overtone order	Fundamental
Motional resistance(ESR)	170 Ω Max. ($24 \leq f < 32$ MHz) 60 Ω Max. ($32 \leq f < 38$ MHz) 50 Ω Max. ($38 \leq f \leq 80$ MHz)
Frequency versus temperature characteristics. (standard)	$\pm 20 \times 10^{-6}$ / -40 °C to +85 °C ($\pm 50 \times 10^{-6}$ / -40 °C to +125 °C)
Frequency Aging	$\pm 1 \times 10^{-6}$ / year Max. ($24 \leq f \leq 54$ MHz) $\pm 3 \times 10^{-6}$ / year Max. ($54 < f \leq 80$ MHz)

❖ Package and Pin Assignments



Added New

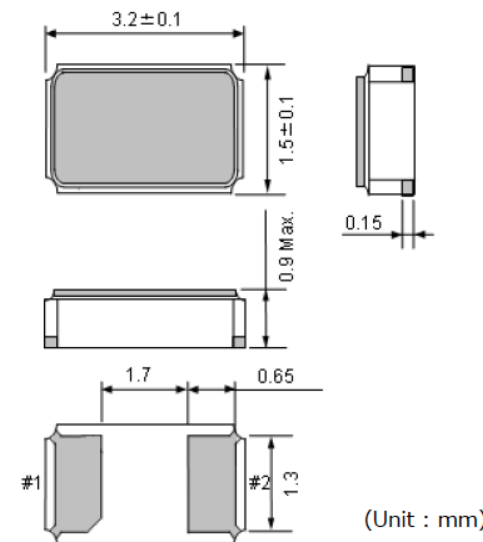
❖ Feature

- Frequency range: 32.768 kHz
- Low ESR: 40 kΩ typ. At +25 °C
- Size: 3.2 x 1.5 x 0.9 t mm
- ✓ Applications: Automotive applications (AEC-Q200)

❖ Overview

Item	Symbol	Specification	Conditions / Remarks
Nominal frequency range	f_nom	32.768 kHz	
Storage temperature	T_stg	-55 °C to +125°C	Storage as single product.
Operating temperature	T_use	-44°C to +125°C	
Level of drive	DL	0.5 μW Max.	
Frequency tolerance	f_tol	$\pm 20 \times 10^{-6}$	+25°C, DL = 0.1μW
Turnover temperature	Ti	+25°C $\pm 5^\circ\text{C}$	
Parabolic coefficient	B	$-0.04 \times 10^{-6} / ^\circ\text{C}^2$ Max.	
Load capacitance	CL	7 pF, 9 pF, 12.5 pF	Please specify
Motional resistance (ESR)	R1	40 kΩ typ. at +25°C 65 kΩ Max. At -40°C + 105°C 70 kΩ Max. At -40°C + 125°C	
Motional capacitance	C1	3.4 fF typ.	
Shunt capacitance	C0	1.0 pF typ.	
Frequency aging	f_age	$\pm 3 \times 10^{-6} / \text{year}$ Max.	+25 °C, First year

❖ External dimensions



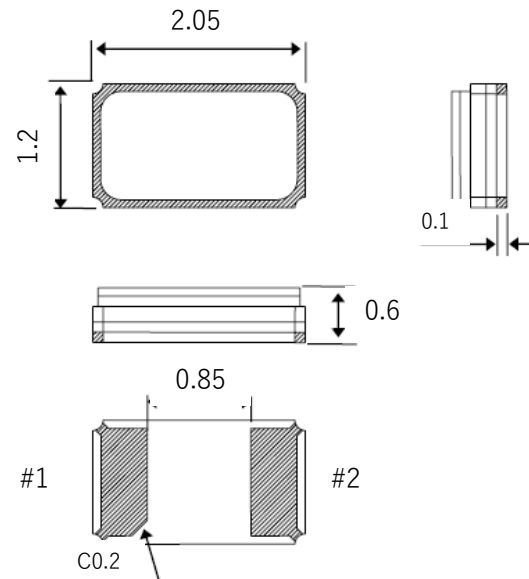
❖ Features

- Low ESR : 40k Ω typ. at +25°C
- Temperature range from -40 to +125°C
- 2012 Package
- AEC-Q200

❖ Specifications:

Item	Symbol	Specifications	Conditions / Remarks
Nominal frequency range	f_nom	32.768 kHz	
Storage temperature	T_stg	-55 °C to +125 °C	Storage as single product.
Operating temperature	T_use	-40 °C to +125 °C	
Level of drive	DL	0.1 μ W (0.5 μ W Max.)	
Frequency tolerance	f_tol	$\pm 20 \times 10^{-6}$	+25 °C, DL=0.1 μ W
Turnover temperature	Ti	+25 °C ± 5 °C	
Parabolic coefficient	B	$-0.04 \times 10^{-6} / ^\circ\text{C}^2$ Max.	
Load capacitance	CL	9 pF, 12.5 pF	Please specify
Motional resistance (ESR)	R1	40 k Ω typ. at +25°C 70 k Ω Max. at -40 to +105°C 75 k Ω Max. at -40 to +125°C	
Motional capacitance	C1	8.4 fF Typ.	
Shunt capacitance	C0	1.6 pF Typ.	
Frequency aging	f_age	$\pm 3 \times 10^{-6} / \text{year}$ Max.	+25 °C, First year

❖ Package and Pin Assignments



❖ Features

- Xtal with integrated thermistor
- Temperature range from -40 to +105 °C
- 2016 Package
- AEC-Q200
- Also available with 38.4 MHz

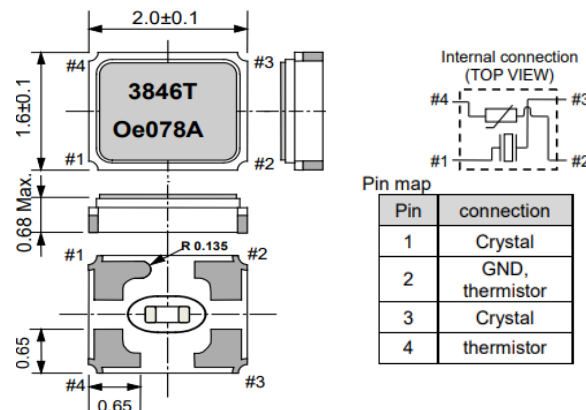
❖ Specifications:

No.	Parameters	Requirements
1	Package type	2.0 x 1.6 mm, t=0.68 mm Max.
2	Nominal frequency	55.200000 MHz
3	Mode of vibration	AT-cut / Fundamental
4	Storage temperature range	-40 to +125 deg.C
5	Operating temperature range	-40 to +105 deg.C
6	Drive level	200 µW Max.
7	Frequency tolerance	± 10 ppm at 25 +/-3 deg.C
8	Frequency versus temperature characteristics	± 20 ppm at -40 to +105 deg.C, Ref. 25 deg.C
9	Frequency aging	± 10 ppm / 10 years at 25 deg.C *2
10	Reflow shift	± 2 ppm / After tow reflows
11	Load capacitance	8.0 pF
12	Equivalent series resistance	50 ohm Max.
13	Insulation resistance	Min. 500 M ohm Min. / DC 100V +/-15V

❖ Applications

- Anti-relay attack smart key for Automotive zone
- Gesture recognition

❖ Package and Pin Assignments



❖ Features

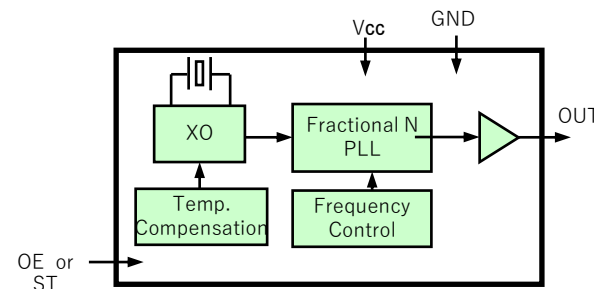
- Any Frequency: accurate to 6 decimal places between 0.67MHz to 170MHz
- High stability LVCMOS output
- Temperature range from -40 to +125 °C
- 2520 Package
- AEC-Q100

❖ Applications

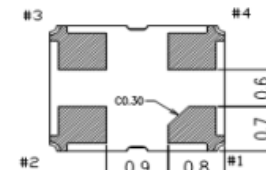
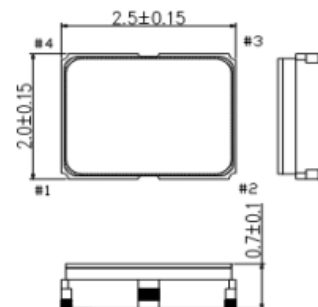
- Camera System, Navigation System, Car network Ethernet

Item	Symbol	Specification
Output Center Frequency range	f _{OUT}	0.67M to 170MHz
Supply voltage	V _{CC}	1.62 V ~ 3.63V
Frequency tolerance (Include variations : initial, temperature, supply voltage, load, reflow, 1year/25°C aging)	f _{TEMP}	+/-15ppm (-40 to 85°C) +/-20ppm (-40 to 105°C) +/-50ppm (-40 to 125°C)
Function of PIN No.1	Func_PIN1	Programmable OE or ST
RMS Phase jitter(170MHz) (12kHz to 20MHz)	tphj(σ)	50 ps typ
RMS Period Jitter(170MHz)	tpej(σ)	2.3 ps typ
Internal Crystal Frequency (f _{OUT} Initial Accuracy)	f _{REF}	26MHz Photo AT (Maximum variation is +/- 1 ppm)
Power Consumption (no load)	I _{DD}	3.4mA Max. (f _{OUT} =20MHz) 7.7mA Max. (f _{OUT} =170MHz) 3.6mA Max. (Output disable) 3.3uA Max. (Stand by)
Package	PKG	2520

❖ Block Diagram



❖ Package and Pin Assignments



Pin #	Connection
#1	OE
#1	ST
#2	GND
#3	OUT
#4	V _{CC}

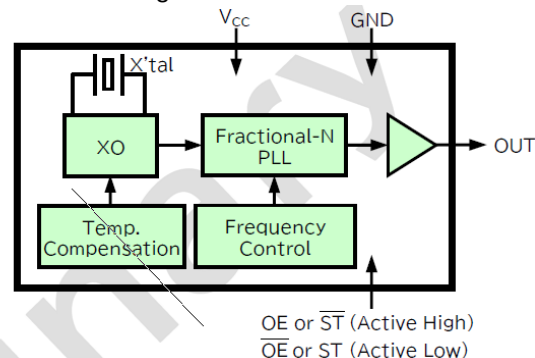
❖ Feature

- Low noise Fractional PLL technology support any frequency
 - Between 1.2 MHz and 170 MHz with quick turn-around time
 - Low jitter characteristics 1.1 ps Typ. at $f_o = 125$ MHz
 - $\pm 15 \times 10^{-6}$ (up to $+105^\circ\text{C}$) / $\pm 25 \times 10^{-6}$ (up to $+125^\circ\text{C}$) with Temperature Compensation function
- AEC-Q100 compliant

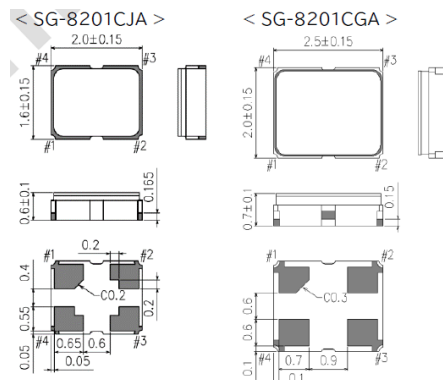
❖ Specifications

Item	Specifications
Frequency (f_o)	1.2 MHz to 170 MHz
Output	CMOS
Supply Voltage (V_{cc})	1.62 V to 3.63 V
Frequency tolerance / Operating temperature	$\pm 15 \times 10^{-6}$ / -40°C to $+105^\circ\text{C}$ $\pm 25 \times 10^{-6}$ / -40°C to $+125^\circ\text{C}$ $\pm 50 \times 10^{-6}$ / -40°C to $+125^\circ\text{C}$ * Includes Initial frequency tolerance, Frequency / temperature characteristics, Frequency / voltage coefficient, Frequency / load coefficient and Aging ($+25^\circ\text{C}$, First year)
Current Consumption (No load)	7.5 mA Max. ($f_o = 25$ MHz) 12.4 mA Max. ($f_o = 125$ MHz)
Symmetry	45% to 55%
Rise/Fall time	2.0 ns Max. ($f_o > 125$ Mhz) 2.5 ns Max. ($75 \text{ MHz} < f_o \leq 125 \text{ Mhz}$) 4.0 ns Max. ($50 \text{ MHz} < f_o \leq 75 \text{ MHz}$) 6.0 ns Max. ($f_o \leq 50 \text{ MHz}$)
Phase Jitter (@125 MHz)	1.1 ps Typ. / 12 kHz to 20 MHz
Function	Output enable or Stand-by

❖ Block diagram



❖ External dimension (unit in mm)



❖ Pin map

#1	OE or $\overline{\text{ST}}$ (Active High) ST or $\overline{\text{OĒ}}$ (Active Low)
#2	GND
#3	OUT
#4	Vcc

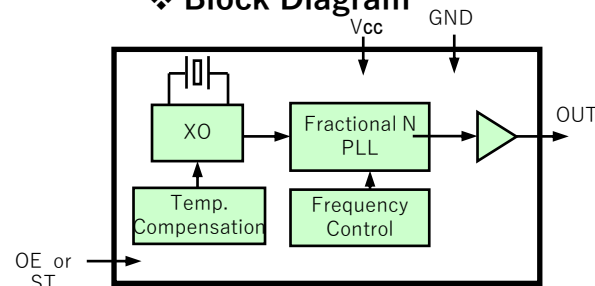
❖ Features

- PLL technology to enable short lead time
- Low jitter 1ps typ. @125MHz
- Temperature range from -40 to +125 °C
- 2016 Package
- AEC-Q100

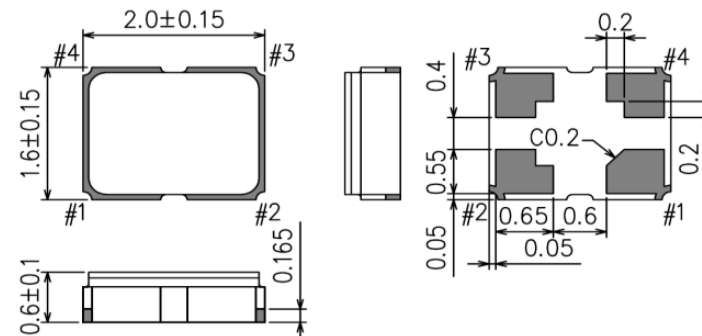
❖ Specification:

Item	Specifications
Output Frequency	1.2MHz to 170MHz
Frequency stability incl. calibration tolerance, temperature, supply voltage variations, reflow drift, load drift and aging	Incl. 1year aging at 25degC +/-15ppm at -40°C~+105°C +/-25ppm at -40°C~+125°C
	Incl. 15years aging at 25degC (approx.) +/-25ppm at -40°C~+105°C +/-35ppm at -40°C~+125°C
Current consumption (No load condition)	5mA Typ.
Supply voltage	1.71V~3.63V
Output	CMOS
Symmetry	45 % to 55 %
Rise / Fall Time (20% to 80%)	2.0ns Max. (125MHz ≤ fo ≤ 170MHz) 2.5ns Max. (75MHz ≤ fo < 125MHz) 4.0ns Max. (50MHz ≤ fo ≤ 75MHz) 6.0ns max. (fo < 50MHz)
Phase jitter (12kHz to 20MHz)	1ps Typ. (125MHz)

❖ Block Diagram



❖ Package and Pin Assignments



home

❖ Applications

Camera System, Navigation System, High Speed Car network

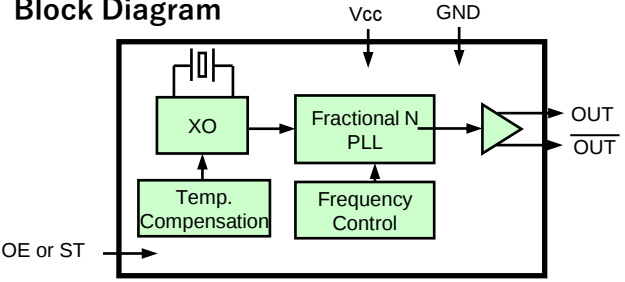
Differential Output Oscillator: SG2520 / 3225C*A

Features

- Conform to AEC-Q100
- Low jitter 0.3 ps Max.
- +/-50 ppm high stability @-40 ° C to +125 ° C
- Output option
 - LVDS with 10 amplitude options
 - includes LVPECL compatible differential amplitude with LVDS termination
 - WA-LVDS, LVPECL, HCSL, LP-HCSL

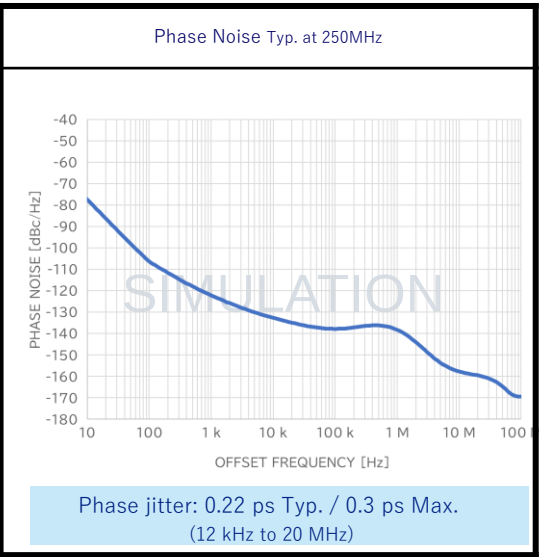
Added New

Block Diagram

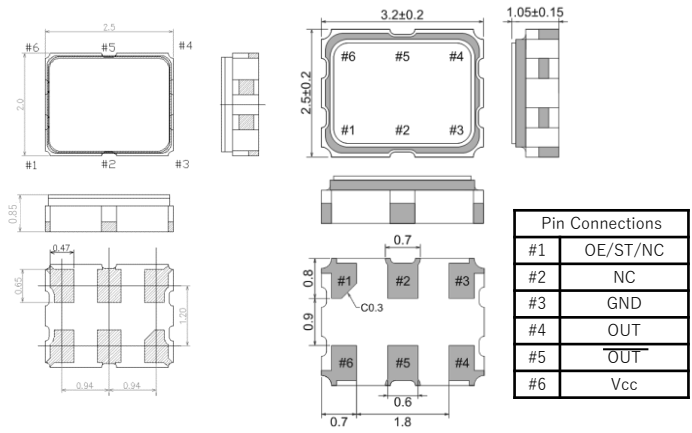


Target Specifications (preliminary)

Item	Specifications
Output Frequency	3.52 MHz to 1000 MHz (NA: 750 to 800MHz)
Frequency stability incl. calibration tolerance, temperature, supply voltage variations, reflow drift, load drift and 10 years aging at +25 ° C.	$\pm 20 \times 10^{-6}$ at -40 ° C to +85 ° C $\pm 25 \times 10^{-6}$ at -40 ° C to +105 ° C $\pm 50 \times 10^{-6}$ at -40 ° C to +125 ° C
Current consumption (Vcc=2.5V, @200MHz)	36 mA Max. LVDS 42 mA Max. LVPECL compatible 38 mA Max. HCSL
Supply voltage	1.71 V to 3.63 V
Symmetry	45 % to 55 %
Phase jitter (12 kHz to 20 MHz)	0.3 ps Max. 0.22 ps Typ. (@268 MHz WA-LVDS)



Package and Pin Assignments



home

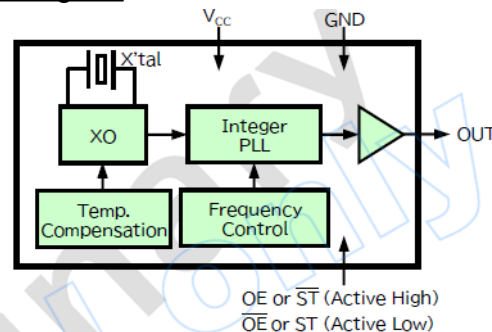
❖ Features

- Low noise Integer PLL technology support
 - Jitter characteristics **0.6 ps Max.** At $f_o=125$ MHz
- $\pm 15 \times 10^{-6}$ (up to $+105^\circ\text{C}$) / $\pm 25 \times 10^{-6}$ (up to $+125^\circ\text{C}$) with Temperature compensation function
- AEC-Q100 compliant

❖ Specifications

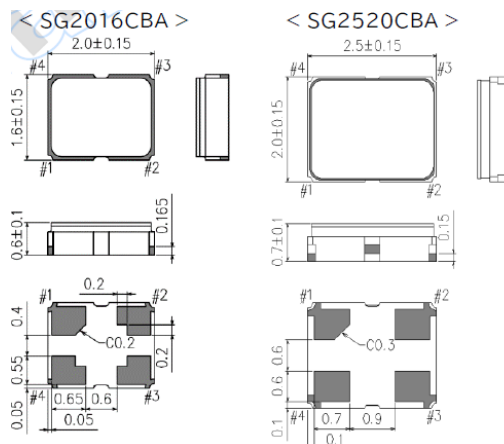
Item	Specification
Standard frequency (f_o)	76.8 MHz / 98.304 MHz / 100 MHz / 125 MHz / 150 MHz / 156.25 MHz
Output	CMOS
Supply voltage (V_{CC})	1.62 V to 3.63 V
Frequency tolerance / Operating temperature	$\pm 15 \times 10^{-6}$ / -40°C to $+105^\circ\text{C}$ $\pm 25 \times 10^{-6}$ / -40°C to $+125^\circ\text{C}$ $\pm 50 \times 10^{-6}$ / -40°C to $+125^\circ\text{C}$ *Including Initial frequency tolerance, Frequency / temperature characteristics, Frequency / voltage coefficient, Frequency / load coefficient and Aging ($+25^\circ\text{C}$, 1 year)
Current Consumption	11.6 mA Max. ($f_o \leq 100\text{MHz}$) 13.2 mA Max. ($100\text{ MHz} < f_o \leq 125\text{ MHz}$) 16.6 mA Max. ($f_o > 125\text{ MHz}$)
Symmetry	45 % to 55%
Rise / Fall Time	2.5 ns Max. ($f_o \leq 125\text{ MHz}$) 2.0 ns Max. ($f_o > 125\text{ MHz}$)
Phase Jitter (@125MHz)	0.6 ps Max. / 12 kHz to 20 MHz
Function	Output enable or Stand-by

❖ Block Diagram



Added New

❖ External Dimension in mm



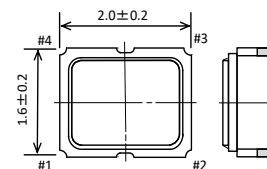
❖ Pin map

#1	OE or $\overline{\text{ST}}$ (Active High) ST or $\overline{\text{OE}}$ (Active Low)
#2	GND
#3	OUT
#4	Vcc

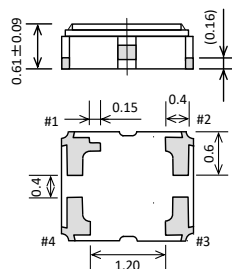
❖ Features

- High stability & Wide temperature range
+/-0.5ppm/-40 to 105°C
- Output Frequency 26 to 55MHz
- Clipped sine wave output
- SMT Package :2.0 x 1.6 x 0.61mm
- AEC-Q100

❖ Package and Pin Assignments



P n	Connection
#1	NC
#2	GND
#3	OUT
#4	VCC



- ❖ Applications:
GNSS, ETC, ADAS, BT

❖ Specifications

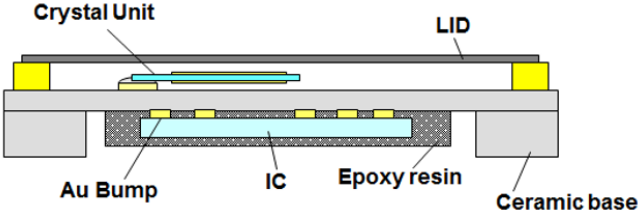
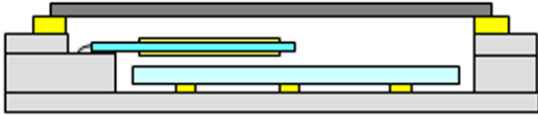
Item	Symbol	Specifications
Output Frequency	f _o	26MHz to 55MHz
Operating temperature	T _{use}	-40°C to +105°C
Supply voltage	V _{cc}	3.3V / 3.0V / 2.8V / 1.8V
Frequency tolerance	f _{tol}	+/-2.0ppm Max. 25°C +/-2°C, After reflow soldering
Frequency / temperature Characteristics	f _o -T _c	+/-0.5ppm Max -40°C to +105°C
Frequency / voltage coefficient	f _o -V _{cc}	+/- 0.2 ppm Max. V _{cc} +/- 5%
Frequency / Load coefficient	f _o -Load	+/- 0.2 ppm Max. 10kΩ//10pF +/-10% each
Frequency aging	f _{age}	+/- 1.0 ppm Max. First year T _{use} = +25° C
Current consumption Output frequency = 26MHz	I _{cc}	2.0mA Max.
Output	OUT	0.8Vpp Min. / load 10kΩ//10pF Clipped sine wave
Symmetry	SYM	40% to 60%
G sensitivity Output frequency = 26MHz	S _g	1.5ppb/G (30Hz to 1.5kHz, sinewave, 3axes)

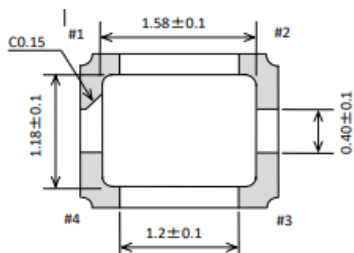
TXCO - TG2016SKA – Technical Advantage



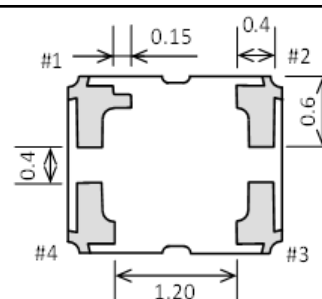
EPSON

The most mentionable advantage of the TG2016SKA in comparison to competitor model is that the integrated thermistor within the semiconductor face same temperature as the Xtal (single cavity).

H-Shape -Competitor	Single Cavity TG2016SKA
	



Equal recommended
foot print





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❖ Features

- Built in 32.768 kHz DTCXO
- High stability (frequency Adjustment)
- Temperature range from -40 to +125 °C
- 3225 Package
- Long Time Availability
- / **RST controller** to detect Vdd drop optional available
- AEC-Q100
- Interface: I2C

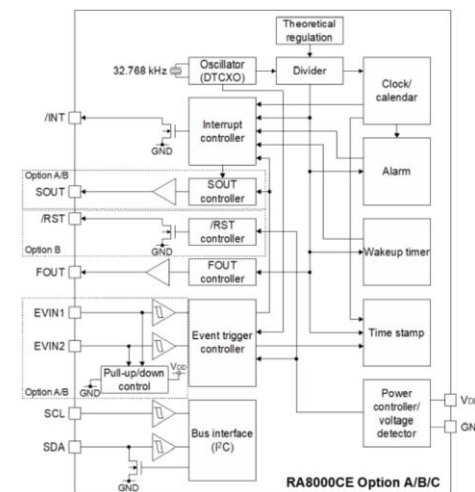
❖ **Specifications:**

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	
Operating voltage	V _{DD}	-		1.6	3.0	5.5	V	
Temp. compensated Voltage	V _{TEM}	-		1.6	3.0	5.5	V	
Clock supply voltage	V _{CLK}	-		1.3	3.0	5.5	V	
Operating temperature	T _a	-		-40	+25	+125	°C	
Frequency tolerance	Δ f / f	YB	T _a = -40 °C to +85 °C	±5.0			x 10 ⁻⁶	
			T _a = +85 °C to +105 °C	±8.0				
			T _a = +105 °C to +125 °C	±50.0				
Current consumption	I _{DD1}	/INT = Hi-Z, FOUT: Output OFF (Hi-Z), Temp. Compensation interval 2.0 s, SCL = SDA = H	No /RST pin	V _{DD} = 5 V	-	0.35	1.8	μA
	I _{DD2}			V _{DD} = 3 V	-	0.3	1.7	
	I _{DD11}		With /RST pin	V _{DD} = 5 V	-	1.5	3.7	
	I _{DD12}			V _{DD} = 2 V	-	0.6	2.25	

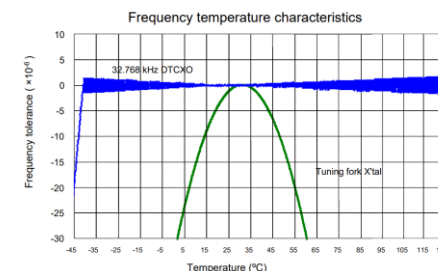
❖ Applications

- Cluster & Infotainment
- Gateway / time sensitive network to control high speed bus systems like LIN,CAN, Ethernet, Flexray

❖ Block Diagram



❖ Temperature compensation



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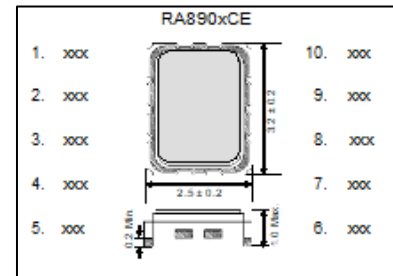
■ Main Features

- Built-in frequency adjusted 32.768 kHz crystal unit and **DTCXO**
- Interface Type : I2C-Bus
- Selectable clock output : 32.768 kHz, 1024 Hz, 1 Hz
- Auto power switching function : Automatically switches to backup power supply by monitoring the V_{DD} voltage
- Alarm interruption : Day, date, hour, minute, second
- Auto repeat wakeup timer interruption
- **AEC-Q100 compliant**
- **Fault detection (Self-monitoring interrupt at crystal oscillation stop)**

■ Specifications

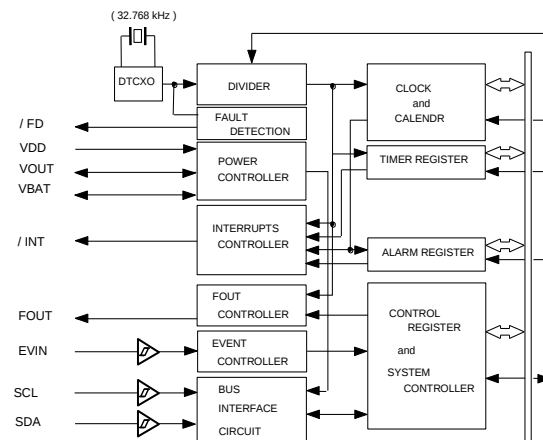
	Item	Symbol	Specs
Operating Conditions	Operating supply voltage	V_{DD}	1.6 V to 5.5 V
	Clock supply voltage	V_{CLK}	1.3 V to 2.5 V
	Operating temperature	T_a	-40 ° C to +125 ° C
Characteristic S	Frequency tolerance	$\Delta f/f$ YB	$\pm 3.4 \times 10^{-6}$ (-40 ° C to 85 ° C) $\pm 8 \times 10^{-6}$ (85 ° C to 105 ° C) $\pm 50 \times 10^{-6}$ (105 ° C to 125 ° C)
	Current consumption	I_{DD2}	350 nA / Typ. 3 V 1800 nA / Max. 3 V (Temp. Compensation interval: 2.0 s)

■ Pin & Function(TBD)



Signal Name	I / O
EVIN	Input
SCL	Input
SDA	Input / Output
FOUT	Output
/INT	Output
/FD	Output
V_{DD}	
V_{OUT}	
V_{BAT}	
GND	

■ Block diagram



■ Schedule
ES : TBD
MP : TBD

Product line-up , Specification (RTC Module)

EPSON

					Planning
Item	RA8900CE	RA8804CE	RA8000CE	RA4000CE	RA890xCE
DTCXO	Yes	Yes	Yes	Yes	Yes
Interface	I ² C	I ² C	I ² C	SPI	I ² C
Operation temp. Max.	+85 ° C	+105 ° C	+125 ° C	+125 ° C	+125 ° C
Frequency tolerance (x 10 ⁻⁶)	UA : ± 3.4 (-40 to +85°C) UB : ± 5.0 (-40 to +85°C)	XA : ± 3.4 (-40 to +85°C) ± 8.0 (+85 to +105°C) XB : ± 5.0 (-40 to +85°C) ± 8.0 (+85 to +105°C)	YB : ± 5.0 (-40 to +85°C) ± 8.0 (+85 to +105°C) ± 50.0 (+105 to +125°C)	YB : ± 5.0 (-40 to +85°C) ± 8.0 (+85 to +105°C) ± 50.0 (+105 to +125°C)	YB : ± 5.0 (-40 to +85°C) ± 8.0 (+85 to +105°C) ± 50.0 (+105 to +125°C)
Backup current Typ. / 3 V	700 nA	350 nA	300 nA	300 nA	350 nA
Time stamp	-	1 time	2 times	2 times	-
Power switching	Yes	-	-	-	Yes
Reset output	-	-	Yes (optional)	Yes (optional)	-
Fault detection (non-recoverable fault)	-	-	-	-	Yes
Automotive grade	AEC-Q200	AEC-Q100	AEC-Q100	AEC-Q100	AEC-Q100

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Global Epson Timing Device

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Reference Design

<https://www.epsondevice.com/crystal/en/techinfo/ic-partners/>

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